

# ARM® CoreLink™ DMC-620 Dynamic Memory Controller

Revision: r0p0

## Technical Reference Manual



**ARM® CoreLink™ DMC-620 Dynamic Memory Controller****Technical Reference Manual**

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**Release information****Document History**

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# Contents

## ARM® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual

### **Preface**

About this book .....	7
Feedback .....	10

### **Chapter 1**

#### **Introduction**

1.1 About the product .....	1-12
1.2 DMC-620 compliance .....	1-13
1.3 Features .....	1-14
1.4 Interfaces .....	1-15
1.5 Configurable options .....	1-16
1.6 Test features .....	1-17
1.7 Product documentation and design flow .....	1-18
1.8 Product revisions .....	1-20

### **Chapter 2**

#### **Functional Description**

2.1 About the functions .....	2-22
2.2 Clocking and resets .....	2-24
2.3 Interfaces .....	2-25
2.4 Constraints and limitations of use .....	2-28

### **Chapter 3**

#### **Programmers Model**

3.1 About this programmers model .....	3-30
--	------

3.2	Register summary .....	3-31
3.3	Register descriptions .....	3-51

## **Appendix A**

### **Signal Descriptions**

A.1	Signals list .....	Appx-A-207
-----	--------------------	------------

## **Appendix B**

### **Revisions**

B.1	Revisions .....	Appx-B-221
-----	-----------------	------------

# Preface

This preface introduces the *ARM® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual*.

It contains the following:

- [About this book on page 7.](#)
- [Feedback on page 10.](#)

## About this book

This book is for the ARM® CoreLink™ DMC-620 Dynamic Memory Controller.

### Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, r1p2, where:

*rm* Identifies the major revision of the product, for example, r1.

*pn* Identifies the minor revision or modification status of the product, for example, p2.

### Intended audience

This book is written for experienced hardware engineers who want to integrate the delivered ARM *System on Chip* (SoC) product in a SoC design.

### Using this book

This book is organized into the following chapters:

#### **Chapter 1 Introduction**

This chapter describes the DMC-620.

#### **Chapter 2 Functional Description**

This chapter describes how the DMC-620 operates.

#### **Chapter 3 Programmers Model**

This chapter describes the programmers model of the DMC-620.

#### **Appendix A Signal Descriptions**

This appendix describes the DMC-620 signals.

#### **Appendix B Revisions**

This appendix describes the technical changes between released issues of this book.

### Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the [ARM Glossary](#) for more information.

### Typographic conventions

*italic*

Introduces special terminology, denotes cross-references, and citations.

**bold**

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

*monospace italic*

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

**monospace bold**

Denotes language keywords when used outside example code.

## <and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments.  
For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

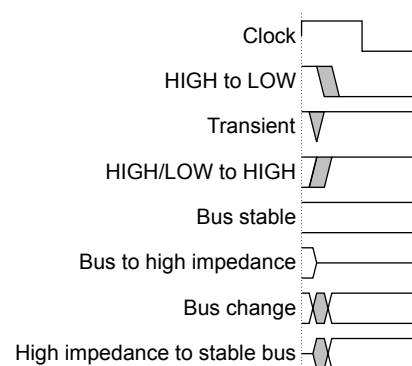
## SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

## Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



**Figure 1 Key to timing diagram conventions**

## Signals

The signal conventions are:

### Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.  
Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

### Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

## Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.



## ARM publications

- *ARM® AMBA® APB Protocol Specification* (ARM IHI 0024).
- *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* (ARM IHI 0068).
- *Principles of ARM® Memory Maps White Paper* (ARM DEN 0001).
- *ARM®v8.2 RAS Architecture Extension Specification*.

The following confidential books are only available to licensees:

- *ARM® CoreLink™ DMC-620 Dynamic Memory Controller Configuration and Integration Manual* (ARM 100569).
- *ARM® CoreLink™ DMC-620 Dynamic Memory Controller Design Manual* (ARM 100567).
- *ARM® CoreLink™ CCN-504 Cache Coherent Network Technical Reference Manual* (ARM 100017).
- *ARM® AMBA® 5 CHI Architecture Specification* (ARM IHI 0050).

## Other publications

- *JEDEC STANDARD DDR3 SDRAM Specification*, JESD79-3D, <http://www.jedec.org>.
- *JEDEC STANDARD DDR3L SDRAM Specification*, JESD79-3-1A, <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 SDRAM Specification*, JESD79-4, <http://www.jedec.org>.
- *JEDEC STANDARD DDR3 RDIMM Specification*, JESD82-29, <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 RDIMM Common Design Specification*, (pre-release), <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 LRDIMM Common Design Specification*, (pre-release), <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 RCD Specification*, (pre-release), <http://www.jedec.org>.
- *JEDEC STANDARD DDR4 DB Specification*, (pre-release), <http://www.jedec.org>.
- *DDR PHY Interface DFI 3.1 Specification*, <http://ddr-phy.org/>.
- *DDR PHY Interface DFI 4.0 Specification*, <http://ddr-phy.org/>.
- *JEDEC STANDARD JESD245 NVDIMM-N Byte Addressable Energy Backed Interface Design Specification*, <http://www.jedec.org>.

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### Note

See the *ARM® CoreLink™ DMC-620 Dynamic Memory Controller Release Note* for the actual versions of the specifications that ARM used when designing the device.

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## Feedback

### Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

### Feedback on content

If you have comments on content then send an e-mail to [errata@arm.com](mailto:errata@arm.com). Give:

- The title *ARM® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual*.
- The number ARM 100568\_0000\_01\_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

————— **Note** —————

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# Chapter 1

## Introduction

This chapter describes the DMC-620.

It contains the following sections:

- *1.1 About the product* on page 1-12.
- *1.2 DMC-620 compliance* on page 1-13.
- *1.3 Features* on page 1-14.
- *1.4 Interfaces* on page 1-15.
- *1.5 Configurable options* on page 1-16.
- *1.6 Test features* on page 1-17.
- *1.7 Product documentation and design flow* on page 1-18.
- *1.8 Product revisions* on page 1-20.

## 1.1 About the product

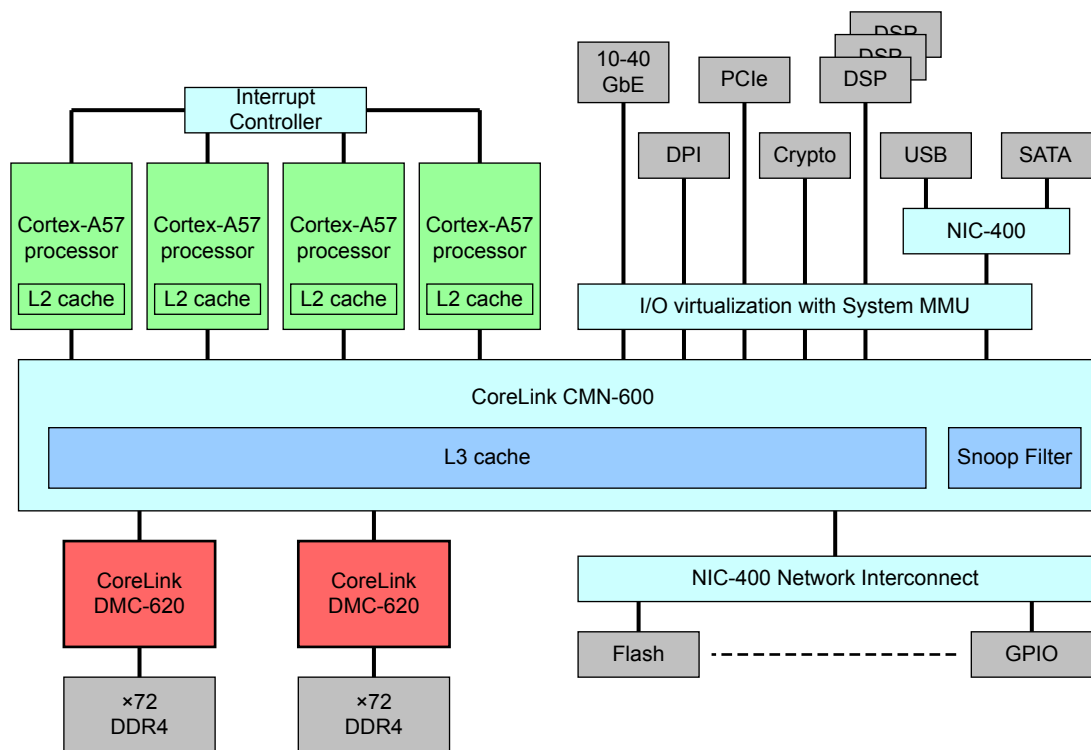
This is a high-level overview of the DMC-620.

The DMC-620 is an ARM AMBA 5 CHI SoC peripheral, developed, tested, and licensed by ARM. It is a high-performance, area-optimized memory controller that is compatible with the AMBA 5 CHI protocol.

It supports the following memory devices:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

The following figure shows an example system:



**Figure 1-1 Example system**

The DMC-620 enables data transfer between the SoC and the SDRAM devices external to the chip. It connects to the on-chip system through a single CHI interface, and to a processor through the programmers APB3 interface to program the DMC-620. It connects to the SDRAM devices through its memory interface block and the *DDR PHY Interface* (DFI).

## 1.2 DMC-620 compliance

The DMC-620 is compatible with the following protocol specifications and standards:

- AMBA 5 CHI enhancement protocol.
- AMBA 3 APB protocol.
- JEDEC DDR4 JESD79-4 standard.
- JEDEC DDR3 JESD79-3 standard.
- JEDEC DDR3L JESD79-3-1 standard.
- JEDEC JESD82-29 standard.
- JEDEC LRDIMM DDR4 Data Buffer DB02 Specification.
- DDR4 RCD02 Specification.
- DDR4 SDRAM Registered DIMM Design Specification.
- DDR4 SDRAM Load Reduced DIMM Design Specification.
- JEDEC JESD245 NVDIMM-N Byte Addressable Energy Backed Interface Specification.
- DFI 3.1.
- DFI 4.0.

## 1.3 Features

The DMC-620 supports DDR3 and DDR4 SDRAMs. It also supports error checking, reliability, availability, and serviceability features. In addition, *Quality of Service* (QoS) features and ARM TrustZone® architecture security extensions are built in throughout the controller.

The DMC-620 has the following features:

- Profiling signals that enable performance profiling to be performed in the system.
- TrustZone architecture security extensions.
- Buffering to optimize read and write turnaround, and to maximize bandwidth.
- A *System Interface* (SI) that provides:
  - A CHI interface to connect to a CoreLink *Cache Coherent Network* (CCN) or a CoreLink *Coherent Mesh Network* (CMN).
  - An AMBA5 CHI interface supporting the CHI-A and CHI-B architecture.
  - An APB interface for configuration and initialization.
  - An external performance event interface for connecting to CoreSight™ on-chip debug and trace technology.
  - A 128-bit or 256-bit CHI interface.
- A *Memory Interface* (MI) that provides:
  - A DFI 3.1 and 4.0 interface to a PHY that supports DDR3, DDR3L, and DDR4.
  - Support for 1:2 DFI frequency ratio mode.
  - Support for either a 32-bit wide data SDRAM interface or a 64-bit wide data SDRAM interface.
- Low-power operation through programmable SDRAM power modes.
- ARMv8.2 compatible *Reliability, Availability, Serviceability* (RAS):
  - *Single Error Correcting, Double Error Detecting* (SECEDED) *Error-Correcting Code* (ECC) for off-chip DRAM.
  - Symbol-based ECC, to correct memory chip and data-lane failures.
  - SECEDED ECC for on-chip RAM protection.
  - Supports ARMv8.2 end-to-end RAS protection, data poisoning, and deferment.
  - Hardware *Read-Modify-Write* (RMW) for systems supporting sparse writes.
  - *Command-Address* (CA) parity checks for DDR3 and DDR4 link faults.
  - CRC write-data protection for DDR4 devices.
- A programmable mechanism for automated SDRAM scrubbing.
- Error handling and automated recovery.
- *Power Control Logic* (PCL) that generates powerdown requests to the SDRAM, and manages power enables for the PHY logic.
- 3DS support for 8H, 4H, and 2H devices.
- DDR4 *Registered Dual In-line Memory Module* (RDIMM) and *Load-Reduced Dual In-line Memory Module* (LRDIMM) support.
- Flexible *Dual In-line Memory Module* (DIMM) topology support:
  - Signal multiplexing that allows a single board layout to support different RDIMM device types (3DS or planer), and a different number of devices.
  - Support for RDIMM Encoded or Direct CS.
  - Core to DMC Prefetch Hint direct path allowing the core to directly initiate a DMC prefetch.
- Configurable out-of-order request queue depth and symbol ECC logic.

## 1.4 Interfaces

This section lists the interfaces in the DMC-620.

The DMC-620 has the following external interfaces:

- A system interface to provide read and write access to or from a master that supports either the CHI-A or CHI-B protocol.
- An APB3 programmers interface to program and control the DMC-620.
- A DFI-compatible PHY interface to transfer data to and from the external memory.
- A profile and debug interface.
- A low-power clock control interface that uses the Q-Channel protocol. See [Q-Channel interface on page 2-26](#).
- An abort interface that is a four-phase request and acknowledge handshake. The abort interface can be used to recover from a livelock when DRAM or PHY fails.
- User I/O ports.
- A set of interrupts that are used to report operational events and detected faults.

## 1.5 Configurable options

The DMC-620 has the following configurable options:

**Table 1-1 Configurable options**

Option	Parameter	Default	Default value	Description
CHI-A or CHI-B	DMC_CHIB	CHIA	0	Configures an AMBA 5 CHI Protocol Specification CHI Issue A or CHI Issue B.
128-bit or 256-bit CHI-B interface	DMC_SYS_DATA_WIDTH	128	128	Valid in CHI-B only. Configures a 128-bit or 256-bit CHI interface.
Include Symbol ECC	DMC_SYM_ECC	Yes	1	Includes logic for Symbol ECC. Symbol ECC is only supported with a x64 DRAM interface.
Queue depth	DMC_QUEUE_DEPTH	128	128	Can select a depth of 64 or 128.

**Note**

- If Symbol ECC is excluded from the configuration, you must ensure the `err0ctlr_ecc` field is never set to 2.
- If the DMC is configured for a CHI-A interconnect, you must ensure the `err0ctlr_cpi` and `err0ctlr_cdi` fields are set to ignore the CHI-B *Data Byte Parity* (DBP) and poison bits.



## 1.6 Test features

The DMC-620 provides the following test features:

- Integration test logic for integration testing.
- A debug and profile interface to enable you to monitor transaction events.

## 1.7 Product documentation and design flow

This section describes the DMC-620 books and how they relate to the design flow.

### Documentation

The DMC-620 documentation is as follows:

#### Technical Reference Manual

The *Technical Reference Manual* (TRM) summarizes the functionality of the DMC, and describes its signals.

The TRM is a non-confidential book available to the public.

#### Design Manual

The *Design Manual* (DM) describes the functionality and the effects of functional options on the behavior of the DMC. It is required at all stages of the design flow. The choices that are made in the design flow mean that some behavior described in the DM is not relevant. If you are programming the DMC, then contact:

- The implementer to determine what integration, if any, was performed before implementing the DMC.
- The integrator to determine the pin configuration of the device that you are using.

The DM is a confidential book that is only available to licensees.

#### Configuration and Integration Manual

The *Configuration and Integration Manual* (CIM) describes how to integrate the DMC into a SoC. The CIM includes a description of the signals that the integrator must tie off to connect the DMC into an SoC design or to other IP.

The CIM describes:

- How to synthesize the *Register Transfer Level* (RTL).
- How to integrate RAM arrays.
- How to run test patterns.
- The processes to sign off the configured design.

The ARM product deliverables include reference scripts and information about using them to implement your design. Contact your EDA vendor for EDA tool support.

The CIM is a confidential book that is only available to licensees.

### Design flow

The DMC-620 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

#### Implementation

The implementer synthesizes the RTL to produce a hard macrocell. This stage includes integrating RAMs into the design.

#### Integration

The integrator connects the implemented design into a SoC. This stage includes connecting it to a memory system.

#### Programming

The system programmer develops the software that is required to initialize the DMC, and tests the required application software.

Each process:

- Can be performed by a different party.
- Can include implementation and integration choices that affect the behavior and features of the DMC.

The operation of the final device depends on:

**Configuration inputs**

The integrator configures some features of the DMC by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

**Software programming**

The programmer configures the DMC by programming particular values into registers. This stage affects the behavior of the DMC.

---

**Note**

This manual refers to implementation-defined features. Reference to a feature that is included means that the appropriate signal configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

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## 1.8 Product revisions

This section describes the differences in functionality between product revisions of the DMC-620.

**r0p0** First release.

# Chapter 2

## Functional Description

This chapter describes how the DMC-620 operates.

It contains the following sections:

- [2.1 About the functions](#) on page 2-22.
- [2.2 Clocking and resets](#) on page 2-24.
- [2.3 Interfaces](#) on page 2-25.
- [2.4 Constraints and limitations of use](#) on page 2-28.

## 2.1 About the functions

This section gives a brief description of all the functions of the DMC-620.

The following figure shows a block diagram of the functions of the DMC-620. The colors show the different categories of functions:

- Blue indicates the blocks that are associated with data flow. The System interface is an example.
- Green indicates the blocks that are associated with programming. The Programming interface is an example.
- Orange indicates the blocks that are associated with the quality and efficiency of the communication to external memory. The QoS engine is an example.

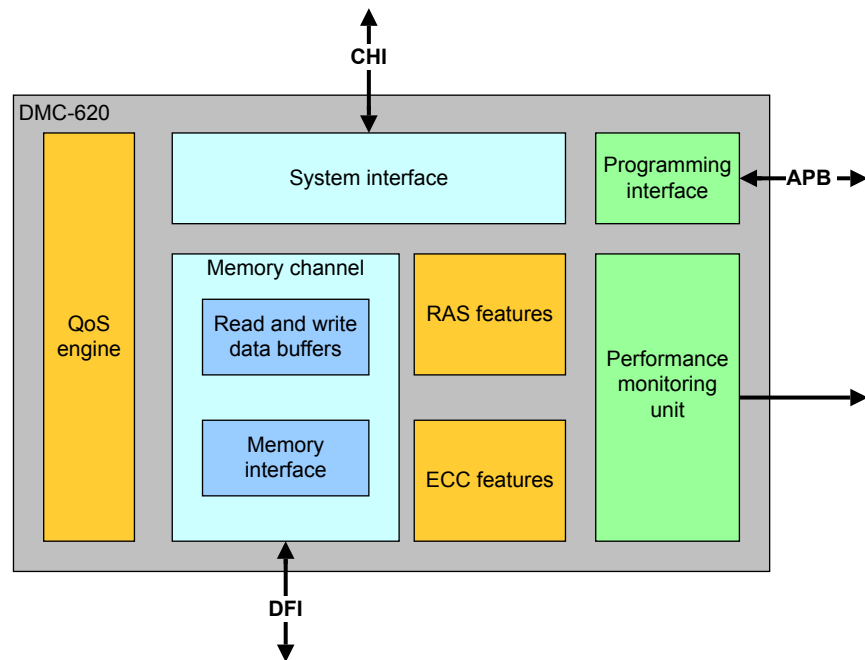


Figure 2-1 DMC functional block diagram

### System Interface

The DMC-620 interfaces to the rest of the SoC through the System Interface. This interface connects to a CHI *Slave Node* (SN-F) interface. For any attempted accesses that the system makes outside of the programmed address range, the System Interface responds with a *Non-data Error* (NDERR) response. Depending on how you program the DMC-620, it converts the system access information to the correct rank, bank, column, and row access of the external SDRAM. The System Interface supports TrustZone features to regulate Secure and Non-secure accesses to both Secure and Non-secure regions of memory.

The DMC monitors queue occupancies and dictates whether system requests of any given QoS are accepted. Prefetched and Dynamic P-Credit requests are allocated based on a threshold setting, which is derived from register settings.

#### Note

There is no support for exclusive access in the DMC because the CoreLink CCN-5xx and CMN-xxx products support exclusive access requests in the *Home Node* (HN-F).

## Memory channel

Through this interface, the DMC-620 conducts data transactions with the SDRAM and regulates the power consumption of the SDRAM. The DMC-620 uses the ECC information that it receives from the SDRAM to maximize the reliability from these devices.

## Programming interface

Through this interface, a master in the system programs the DMC-620. You can define the Secure and Non-secure regions of external memory and also define how the DMC-620 addresses the external memory from the address that the system provides on its System interface. You can also make direct accesses to the SDRAM, for example to initialize it.

## QoS engine

The DMC-620 provides controls to enable you to adjust its arbitration scheme for your system to maximize the availability of your external memory devices. It provides buffers to re-order system transaction requests. It uses an advanced scheduling algorithm to ensure that traffic going to one memory bank causes minimal disruption to traffic going to a different memory bank. It also schedules transaction requests according to the availability of the destination memory bank. For system access requests to different available memory banks, the DMC-620 arbitrates these requests using the QoS priority initially, and then the temporal priority. These memory access requests all compete for control of the external SDRAM bus and SDRAM bank.

## RAS

RAS features include support for the following:

- V8.2 RAS Extension compliant.
- Supports end-to-end RAS protection, data poisoning, and deferment.
- SECDED ECC and symbol-based ECC for external DRAM. The symbol-based ECC performs quad-symbol correct and multi-symbol detect.
- SECDED ECC of on-chip SRAM buffers within the DMC-620.
- An automated retry of failed read transactions.
- Write-back of corrected errors.
- To improve containment of faults, the DMC-620 supports:
  - Link error protection for the memory interface, including automated hardware recovery for system memory access, training, and other hardware operations.
  - Programmable data scrubbing. The DMC-620 periodically detects and corrects data errors in the memory autonomously.

## 2.2 Clocking and resets

The DMC-620 normally operates as one synchronous clock domain between the interconnect and the external DDR interface. However, the programming interface can operate asynchronously to this.

This section shows the clock and reset signals that the DMC-620 requires.

### Clocks

There are either two or three clock inputs depending on the DFI frequency ratio configuration:

- **clk**. This is the main DMC clock that runs at SDRAM clock frequency. It must run synchronous to, and at the same frequency, as the CHI interface. If the CHI interface is not running at SDRAM clock frequency, then a *Device Source Synchronous Bridge* (DSSB), which is part of the CCN product must be used. When in a 1:1 DFI frequency ratio mode, this clock also serves as the **dfi clk**.
- **dfi\_clk**. This clock port only exists if the DMC is in 1:2 or 1:4 mode. The clock runs the DFI interface and connects to both the DMC and the PHY. It must be edge synchronous to **clk**, and run at half the **clk** frequency if it is in the 1:2 configuration or one quarter the **clk** frequency when in the 1:4 configuration.
- **pclk**. This can run asynchronously to **clk** and **dfi clk**.

### Reset

Resets must be applied for a minimum duration of 16 clock cycles for each clock domain.

There are two reset inputs. **RESETn** resets both **clk** and **dfi clk** registers and **PRESETn** resets **pclk** registers. The **pclk** domain must be brought out of reset prior to the **clk** and **dfi clk** domains.

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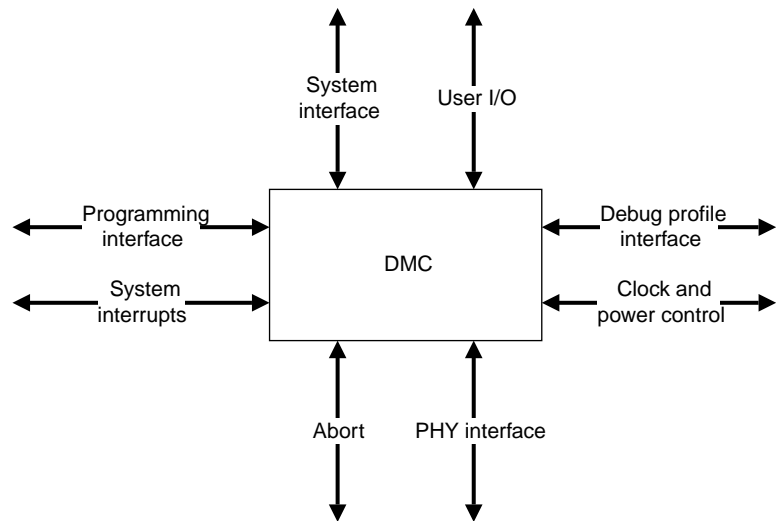
#### Note

- To assert any DMC-620 reset signal, you must set it LOW.
  - To perform a DMC-620 reset, you must assert both reset signals.
-



## 2.3 Interfaces

This section describes the interfaces of the DMC-620, as the following figure shows.



**Figure 2-2 Interfaces of the DMC-620**

This section contains the following subsections:

- [2.3.1 System interface on page 2-25.](#)
- [2.3.2 Programming interface on page 2-25.](#)
- [2.3.3 PHY interface on page 2-25.](#)
- [2.3.4 Profile and debug interface on page 2-26.](#)
- [2.3.5 Low-power clock control interface on page 2-26.](#)
- [2.3.6 Abort interface on page 2-27.](#)

### 2.3.1 System interface

This section describes the function of the System interface.

The System Interface provides protocol conversion between CHI and internal read/write requests. Because CHI is packet-based, and a slave node only supports read and write semantics, this translation is straightforward at a transaction level because no transformation function is performed.

### 2.3.2 Programming interface

This section describes the APB3 interface, which is used for programming the DMC-620.

The AMBA APB3 slave interface allows software to configure the controller and to initialize the memory devices. The APB3 programming interface also provides a means of performing architectural state transitions in addition to querying certain debug and profile information. The APB3 interface is a memory-mapped register interface.

### 2.3.3 PHY interface

The PHY interface provides command scheduling and arbitration, including the generation of any required SDRAM prepare commands, for example, ACTIVATE and PRECHARGE.

The PHY interface is compatible with the DDR standards for DDR4 and DDR3 (including DDR3L). It provides:

- Command scheduling and arbitration.
- Automated AUTOREFRESH command generation.

- SDRAM interface link protection including automated retries for failed commands to ensure the correct ordering of those retried commands to SDRAM.
- Automated SDRAM and PHY logic power control.
- Profile and debug information.
- Support for 1:2 frequency ratio mode.

### 2.3.4 Profile and debug interface

This section describes the profile and debug interface in the DMC-620.

The DMC-620 provides programmable features that allow system designers and software developers to fine-tune performance and power settings for their applications. Several events can be monitored and the statistics that are used to enhance the performance of the controller by statically, or dynamically, altering the programmed state.

The information is made available through output pins that the system integrator must connect to an external monitoring unit.

The following events are monitored:

- Channel utilization.
- Channel and chip power state information.
- Bank utilization.
- Bank distribution.
- Activation rate.
- Read and write turnaround frequency.
- Read and write buffer fill status and the frequency of full events.
- Thresholding asserting back pressure.
- Arbitration decisions where QoS is prioritized over efficiency.
- *Read-Modify-Write* (RMW) frequency.
- Timeouts and deadline events.

Each event is implemented as a pair of signals, VALID, and either PAYLOAD or a permanently valid PAYLOAD signal.

The profile and debug interface can be connected to a generic event counter block. Connecting to a generic event counter block enables any combination of the signals can be logged and tracked, depending on your system requirements.

### 2.3.5 Low-power clock control interface

This section describes the clock requirements for the DMC-620.

The DMC-620 provides a low-power control interface using the Q-Channel protocol. The low-power control interface is used to place the DMC into its low-power state, where the clock can be removed. The system can use the APB interface to put the DMC into its low-power state, and take it out of its low-power state.

#### Q-Channel interface

The DMC has a Q-Channel interface that allows an external power controller to place the DMC into a low-power state.

It is a standard Q-Channel interface as defined in the *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* using the following signals:

- **qactive**.
- **qreqn**.
- **qacceptn**.
- **qdeny**.

When the DMC receives a request, it puts the DRAM into self\_refresh before asserting **qacceptn** to accept the request that indicates the **clk** can be stopped.

The DMC denies requests to power down using the Q-Channel when `geardown_mode` is enabled. In this case, low-power mode can still be entered using the APB interface.

There is a separate Q-Channel interface for the **pclk** using the following signals:

- **qactive\_apb.**
- **qreqn\_apb.**
- **qacceptn\_apb.**
- **qdeny\_apb.**

The DMC never denies a request to power down the APB clock although it might be delayed based on APB activity.

————— **Note** —————

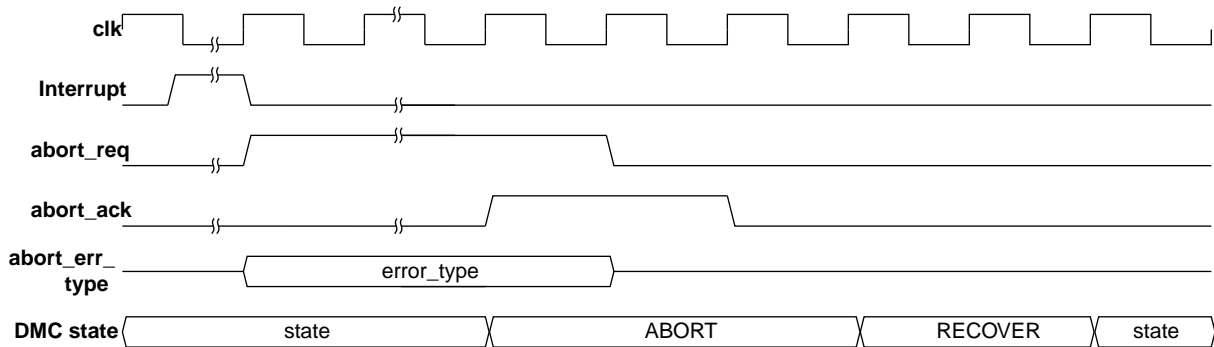
These two interfaces are interrelated and a change on one can cause **qactive** on the other to be asserted. If this occurs, then the powerup request must be responded to in a timely fashion to allow the request to be serviced.

See *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces*.

### 2.3.6 Abort interface

When a fault is detected on the DFI interface, it causes repeated retries of commands on the memory interface. The abort interface is a 4-phase request and acknowledge handshake that the DMC can use to recover from a livelock that is caused by a DRAM failure or a PHY failure.

The following diagram shows the request, acknowledge handshake:



**Figure 2-3 Abort interface timing diagram**

The system can issue an abort at any time, which puts the DMC into the ABORT architectural state. Software must then restore the memory state. All current system transactions are retried after software restores the memory state and puts the DMC back into the READY state.

The abort interface has the payload signal **abort\_err\_type** as an input to the DMC, which the DMC outputs as **dfi\_disconnect\_error** on the DFI interface during an abort sequence. Any PHY training that is in progress gets aborted and the DMC indicates to the PHY the error type through **dfi\_disconnect\_error**. See the DFI4.0 DFI Disconnect in for more information.

## 2.4 Constraints and limitations of use

The constraints and limitations of the DMC-620 depend on the SDRAMs used, and the interoperability within the PHYs. This, in turn, depends on the *DDR Physical Interface* (DFI) parameters.

The SDRAMs supported by the DMC-620 are:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

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### Note

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These devices are described in the JEDEC specifications that are global standards for the microelectronics industry.

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The DIMMs supported by the DMC-620 are:

- DDR3 UDIMM.
- DDR4 UDIMM.
- DDR4 RDIMM.
- DDR4 LRDIMM.
- DDR4 3DS. DIMMs utilizing 3DS parts are supported.

The JEDEC specification implies the following constraints and must be met:

1.  $t_{xp} < t_{xsr}$  - Exiting power down timing must be less than self-refresh exit.
2.  $t_{mrw\_cs} < t_{mrw}$  - The delay after a Mode Register Write command and before any other command is issued to a different rank less than the delay applied after a Mode Register Write command and before any other command is issued to the same rank.

# Chapter 3

## Programmers Model

This chapter describes the programmers model of the DMC-620.

It contains the following sections:

- [3.1 About this programmers model on page 3-30.](#)
- [3.2 Register summary on page 3-31.](#)
- [3.3 Register descriptions on page 3-51.](#)

## 3.1 About this programmers model

The following information applies to the dmc620 registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to the reset value specified in the [3.2 Register summary on page 3-31](#)
- Access type is described as follows:

**RW**      Read and write.

**RO**      Read only.

**WO**      Write only.

## 3.2 Register summary

The following table shows the registers in offset order from the base memory address.

**Table 3-1 Register summary**

Offset	Name	Type	Reset	Width	Description
0x000	memc_status	RO	0x00000000	32	<a href="#">3.3.1 memc_status</a> on page 3-51
0x004	memc_config	RO	0x00000000	32	<a href="#">3.3.2 memc_config</a> on page 3-51
0x008	memc_cmd	WO	0x00000000	32	<a href="#">3.3.3 memc_cmd</a> on page 3-51
0x010	address_control_next	RW	0x00030202	32	<a href="#">3.3.4 address_control_next</a> on page 3-52
0x014	decode_control_next	RW	0x001A3000	32	<a href="#">3.3.5 decode_control_next</a> on page 3-52
0x018	format_control	RW	0x12000113	32	<a href="#">3.3.6 format_control</a> on page 3-52
0x01C	address_map_next	RW	0x00000000	32	<a href="#">3.3.7 address_map_next</a> on page 3-53
0x020	low_power_control_next	RW	0x00000020	32	<a href="#">3.3.8 low_power_control_next</a> on page 3-53
0x028	turnaround_control_next	RW	0x0F0F0F0F	32	<a href="#">3.3.9 turnaround_control_next</a> on page 3-53
0x02C	hit_turnaround_control_next	RW	0x08909FBF	32	<a href="#">3.3.10 hit_turnaround_control_next</a> on page 3-53
0x030	qos_class_control_next	RW	0x0000FC8	32	<a href="#">3.3.11 qos_class_control_next</a> on page 3-54
0x034	escalation_control_next	RW	0x00080F03	32	<a href="#">3.3.12 escalation_control_next</a> on page 3-54
0x038	qv_control_31_00_next	RW	0x76543210	32	<a href="#">3.3.13 qv_control_31_00_next</a> on page 3-54
0x03C	qv_control_63_32_next	RW	0xFEDCBA98	32	<a href="#">3.3.14 qv_control_63_32_next</a> on page 3-55
0x040	rt_control_31_00_next	RW	0x00000000	32	<a href="#">3.3.15 rt_control_31_00_next</a> on page 3-55
0x044	rt_control_63_32_next	RW	0x00000000	32	<a href="#">3.3.16 rt_control_63_32_next</a> on page 3-55
0x048	timeout_control_next	RW	0x00000001	32	<a href="#">3.3.17 timeout_control_next</a> on page 3-56
0x04C	credit_control_next	RW	0x0000F03	32	<a href="#">3.3.18 credit_control_next</a> on page 3-56
0x050	write_priority_control_31_00_next	RW	0x00000000	32	<a href="#">3.3.19 write_priority_control_31_00_next</a> on page 3-56
0x054	write_priority_control_63_32_next	RW	0x00000000	32	<a href="#">3.3.20 write_priority_control_63_32_next</a> on page 3-56
0x058	queue_threshold_control_31_00_next	RW	0x00000008	32	<a href="#">3.3.21 queue_threshold_control_31_00_next</a> on page 3-57
0x05C	queue_threshold_control_63_32_next	RW	0x00000000	32	<a href="#">3.3.22 queue_threshold_control_63_32_next</a> on page 3-57
0x060	address_shutter_31_00_next	RW	0x00000000	32	<a href="#">3.3.23 address_shutter_31_00_next</a> on page 3-57
0x064	address_shutter_63_32_next	RW	0x00000000	32	<a href="#">3.3.24 address_shutter_63_32_next</a> on page 3-58
0x068	address_shutter_95_64_next	RW	0x00000000	32	<a href="#">3.3.25 address_shutter_95_64_next</a> on page 3-58
0x06C	address_shutter_127_96_next	RW	0x00000000	32	<a href="#">3.3.26 address_shutter_127_96_next</a> on page 3-58
0x070	address_shutter_159_128_next	RW	0x00000000	32	<a href="#">3.3.27 address_shutter_159_128_next</a> on page 3-59
0x074	address_shutter_191_160_next	RW	0x00000000	32	<a href="#">3.3.28 address_shutter_191_160_next</a> on page 3-59

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x078	memory_address_max_31_00_next	RW	0x00000010	32	<a href="#">3.3.29 memory_address_max_31_00_next</a> on page 3-59
0x07C	memory_address_max_47_32_next	RW	0x00000000	32	<a href="#">3.3.30 memory_address_max_47_32_next</a> on page 3-59
0x080	access_address_min0_31_00_next	RW	0x00000000	32	<a href="#">3.3.31 access_address_min0_31_00_next</a> on page 3-60
0x084	access_address_min0_47_32_next	RW	0x00000000	32	<a href="#">3.3.32 access_address_min0_47_32_next</a> on page 3-60
0x088	access_address_max0_31_00_next	RW	0x00000000	32	<a href="#">3.3.33 access_address_max0_31_00_next</a> on page 3-60
0x08C	access_address_max0_47_32_next	RW	0x00000000	32	<a href="#">3.3.34 access_address_max0_47_32_next</a> on page 3-61
0x090	access_address_min1_31_00_next	RW	0x00000000	32	<a href="#">3.3.35 access_address_min1_31_00_next</a> on page 3-61
0x094	access_address_min1_47_32_next	RW	0x00000000	32	<a href="#">3.3.36 access_address_min1_47_32_next</a> on page 3-61
0x098	access_address_max1_31_00_next	RW	0x00000000	32	<a href="#">3.3.37 access_address_max1_31_00_next</a> on page 3-62
0x09C	access_address_max1_47_32_next	RW	0x00000000	32	<a href="#">3.3.38 access_address_max1_47_32_next</a> on page 3-62
0x0A0	access_address_min2_31_00_next	RW	0x00000000	32	<a href="#">3.3.39 access_address_min2_31_00_next</a> on page 3-62
0x0A4	access_address_min2_47_32_next	RW	0x00000000	32	<a href="#">3.3.40 access_address_min2_47_32_next</a> on page 3-62
0x0A8	access_address_max2_31_00_next	RW	0x00000000	32	<a href="#">3.3.41 access_address_max2_31_00_next</a> on page 3-63
0x0AC	access_address_max2_47_32_next	RW	0x00000000	32	<a href="#">3.3.42 access_address_max2_47_32_next</a> on page 3-63
0x0B0	access_address_min3_31_00_next	RW	0x00000000	32	<a href="#">3.3.43 access_address_min3_31_00_next</a> on page 3-63
0x0B4	access_address_min3_47_32_next	RW	0x00000000	32	<a href="#">3.3.44 access_address_min3_47_32_next</a> on page 3-64
0x0B8	access_address_max3_31_00_next	RW	0x00000000	32	<a href="#">3.3.45 access_address_max3_31_00_next</a> on page 3-64
0x0BC	access_address_max3_47_32_next	RW	0x00000000	32	<a href="#">3.3.46 access_address_max3_47_32_next</a> on page 3-64
0x0C0	access_address_min4_31_00_next	RW	0x00000000	32	<a href="#">3.3.47 access_address_min4_31_00_next</a> on page 3-65
0x0C4	access_address_min4_47_32_next	RW	0x00000000	32	<a href="#">3.3.48 access_address_min4_47_32_next</a> on page 3-65
0x0C8	access_address_max4_31_00_next	RW	0x00000000	32	<a href="#">3.3.49 access_address_max4_31_00_next</a> on page 3-65



Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0CC	access_address_max4_47_32_next	RW	0x00000000	32	<a href="#">3.3.50 access_address_max4_47_32_next</a> on page 3-65
0x0D0	access_address_min5_31_00_next	RW	0x00000000	32	<a href="#">3.3.51 access_address_min5_31_00_next</a> on page 3-66
0x0D4	access_address_min5_47_32_next	RW	0x00000000	32	<a href="#">3.3.52 access_address_min5_47_32_next</a> on page 3-66
0x0D8	access_address_max5_31_00_next	RW	0x00000000	32	<a href="#">3.3.53 access_address_max5_31_00_next</a> on page 3-66
0x0DC	access_address_max5_47_32_next	RW	0x00000000	32	<a href="#">3.3.54 access_address_max5_47_32_next</a> on page 3-67
0x0E0	access_address_min6_31_00_next	RW	0x00000000	32	<a href="#">3.3.55 access_address_min6_31_00_next</a> on page 3-67
0x0E4	access_address_min6_47_32_next	RW	0x00000000	32	<a href="#">3.3.56 access_address_min6_47_32_next</a> on page 3-67
0x0E8	access_address_max6_31_00_next	RW	0x00000000	32	<a href="#">3.3.57 access_address_max6_31_00_next</a> on page 3-68
0x0EC	access_address_max6_47_32_next	RW	0x00000000	32	<a href="#">3.3.58 access_address_max6_47_32_next</a> on page 3-68
0x0F0	access_address_min7_31_00_next	RW	0x00000000	32	<a href="#">3.3.59 access_address_min7_31_00_next</a> on page 3-68
0x0F4	access_address_min7_47_32_next	RW	0x00000000	32	<a href="#">3.3.60 access_address_min7_47_32_next</a> on page 3-68
0x0F8	access_address_max7_31_00_next	RW	0x00000000	32	<a href="#">3.3.61 access_address_max7_31_00_next</a> on page 3-69
0x0FC	access_address_max7_47_32_next	RW	0x00000000	32	<a href="#">3.3.62 access_address_max7_47_32_next</a> on page 3-69
0x100	channel_status	RO	0x00000003	32	<a href="#">3.3.63 channel_status</a> on page 3-69
0x104	channel_status_63_32	RO	0x00000000	32	<a href="#">3.3.64 channel_status_63_32</a> on page 3-70
0x108	direct_addr	RW	0x00000000	32	<a href="#">3.3.65 direct_addr</a> on page 3-70
0x10C	direct_cmd	WO	0x00000000	32	<a href="#">3.3.66 direct_cmd</a> on page 3-70
0x110	dci_replay_type_next	RW	0x00000002	32	<a href="#">3.3.67 dci_replay_type_next</a> on page 3-71
0x114	direct_control_next	RW	0x0003FFFF	32	<a href="#">3.3.68 direct_control_next</a> on page 3-71
0x118	dci_strb	RW	0x0000000F	32	<a href="#">3.3.69 dci_strb</a> on page 3-71
0x11C	dci_data	RW	0x00000000	32	<a href="#">3.3.70 dci_data</a> on page 3-71
0x120	refresh_control_next	RW	0x00000000	32	<a href="#">3.3.71 refresh_control_next</a> on page 3-72
0x128	memory_type_next	RW	0x00000101	32	<a href="#">3.3.72 memory_type_next</a> on page 3-72
0x130	feature_config	RW	0x000018E0	32	<a href="#">3.3.73 feature_config</a> on page 3-72
0x138	nibble_failed_031_000	RW	0x00000000	32	<a href="#">3.3.74 nibble_failed_031_000</a> on page 3-73
0x13C	nibble_failed_063_032	RW	0x00000000	32	<a href="#">3.3.75 nibble_failed_063_032</a> on page 3-73

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x140	nibble_failed_095_064	RW	0x00000000	32	<a href="#">3.3.76 nibble_failed_095_064</a> on page 3-73
0x144	nibble_failed_127_096	RW	0x00000000	32	<a href="#">3.3.77 nibble_failed_127_096</a> on page 3-74
0x148	queue_allocate_control_031_000	RW	0xFFFFFFFF	32	<a href="#">3.3.78 queue_allocate_control_031_000</a> on page 3-74
0x14C	queue_allocate_control_063_032	RW	0xFFFFFFFF	32	<a href="#">3.3.79 queue_allocate_control_063_032</a> on page 3-74
0x150	queue_allocate_control_095_064	RW	0xFFFFFFFF	32	<a href="#">3.3.80 queue_allocate_control_095_064</a> on page 3-75
0x154	queue_allocate_control_127_096	RW	0xFFFFFFFF	32	<a href="#">3.3.81 queue_allocate_control_127_096</a> on page 3-75
0x16C	link_err_count	RW	0x00000000	32	<a href="#">3.3.82 link_err_count</a> on page 3-75
0x170	scrub_control0_next	RW	0x0FFFFFF0	32	<a href="#">3.3.83 scrub_control0_next</a> on page 3-76
0x174	scrub_address_min0_next	RW	0x00000000	32	<a href="#">3.3.84 scrub_address_min0_next</a> on page 3-76
0x178	scrub_address_max0_next	RW	0x00000000	32	<a href="#">3.3.85 scrub_address_max0_next</a> on page 3-76
0x17C	scrub_address_current0	RO	0x00000000	32	<a href="#">3.3.86 scrub_address_current0</a> on page 3-76
0x180	scrub_control1_next	RW	0x0FFFFFF0	32	<a href="#">3.3.87 scrub_control1_next</a> on page 3-77
0x184	scrub_address_min1_next	RW	0x00000000	32	<a href="#">3.3.88 scrub_address_min1_next</a> on page 3-77
0x188	scrub_address_max1_next	RW	0x00000000	32	<a href="#">3.3.89 scrub_address_max1_next</a> on page 3-77
0x18C	scrub_address_current1	RO	0x00000000	32	<a href="#">3.3.90 scrub_address_current1</a> on page 3-78
0x1A0	cs_remap_control_31_00_next	RW	0x00020001	32	<a href="#">3.3.91 cs_remap_control_31_00_next</a> on page 3-78
0x1A4	cs_remap_control_63_32_next	RW	0x00080004	32	<a href="#">3.3.92 cs_remap_control_63_32_next</a> on page 3-78
0x1A8	cs_remap_control_95_64_next	RW	0x00200010	32	<a href="#">3.3.93 cs_remap_control_95_64_next</a> on page 3-79
0x1AC	cs_remap_control_127_96_next	RW	0x00800040	32	<a href="#">3.3.94 cs_remap_control_127_96_next</a> on page 3-79
0x1B0	cid_remap_control_31_00_next	RW	0x20001000	32	<a href="#">3.3.95 cid_remap_control_31_00_next</a> on page 3-79
0x1B4	cid_remap_control_63_32_next	RW	0x00004000	32	<a href="#">3.3.96 cid_remap_control_63_32_next</a> on page 3-79
0x1C0	cke_remap_control_next	RW	0x76543210	32	<a href="#">3.3.97 cke_remap_control_next</a> on page 3-80
0x1C4	rst_remap_control_next	RW	0x76543210	32	<a href="#">3.3.98 rst_remap_control_next</a> on page 3-80
0x1C8	ck_remap_control_next	RW	0x76543210	32	<a href="#">3.3.99 ck_remap_control_next</a> on page 3-80
0x1D0	power_group_control_31_00_next	RW	0x00020001	32	<a href="#">3.3.100 power_group_control_31_00_next</a> on page 3-81
0x1D4	power_group_control_63_32_next	RW	0x00080004	32	<a href="#">3.3.101 power_group_control_63_32_next</a> on page 3-81
0x1D8	power_group_control_95_64_next	RW	0x00200010	32	<a href="#">3.3.102 power_group_control_95_64_next</a> on page 3-81
0x1DC	power_group_control_127_96_next	RW	0x00800040	32	<a href="#">3.3.103 power_group_control_127_96_next</a> on page 3-82
0x1E0	phy_rdwrdata_cs_mask_31_00	RW	0xF7FBDFE	32	<a href="#">3.3.104 phy_rdwrdata_cs_mask_31_00</a> on page 3-82

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1E4	phy_rdwrddata_cs_mask_63_32	RW	0x7FBFDFEF	32	3.3.105 <i>phy_rdwrddata_cs_mask_63_32</i> on page 3-82
0x1E8	phy_request_cs_remap	RW	0x76543210	32	3.3.106 <i>phy_request_cs_remap</i> on page 3-83
0x1F0	feature_control_next	RW	0x0AA00000	32	3.3.107 <i>feature_control_next</i> on page 3-83
0x1F4	mux_control_next	RW	0x00000000	32	3.3.108 <i>mux_control_next</i> on page 3-83
0x1F8	rank_remap_control_next	RW	0x76543210	32	3.3.109 <i>rank_remap_control_next</i> on page 3-84
0x200	t_refi_next	RW	0x00090100	32	3.3.110 <i>t_refi_next</i> on page 3-84
0x204	t_rfc_next	RW	0x00008C23	32	3.3.111 <i>t_rfc_next</i> on page 3-84
0x208	t_mrr_next	RW	0x00000002	32	3.3.112 <i>t_mrr_next</i> on page 3-84
0x20C	t_mrw_next	RW	0x0000000C	32	3.3.113 <i>t_mrw_next</i> on page 3-85
0x218	t_rcd_next	RW	0x00000005	32	3.3.114 <i>t_rcd_next</i> on page 3-85
0x21C	t_ras_next	RW	0x0000000E	32	3.3.115 <i>t_ras_next</i> on page 3-86
0x220	t_rp_next	RW	0x00000005	32	3.3.116 <i>t_rp_next</i> on page 3-86
0x224	t_rpall_next	RW	0x00000005	32	3.3.117 <i>t_rpall_next</i> on page 3-86
0x228	t_rrd_next	RW	0x04000404	32	3.3.118 <i>t_rrd_next</i> on page 3-87
0x22C	t_act_window_next	RW	0x03561414	32	3.3.119 <i>t_act_window_next</i> on page 3-87
0x234	t_rtr_next	RW	0x10060404	32	3.3.120 <i>t_rtr_next</i> on page 3-87
0x238	t_rtw_next	RW	0x00060606	32	3.3.121 <i>t_rtw_next</i> on page 3-88
0x23C	t_rtp_next	RW	0x00000004	32	3.3.122 <i>t_rtp_next</i> on page 3-88
0x244	t_wr_next	RW	0x00000005	32	3.3.123 <i>t_wr_next</i> on page 3-88
0x248	t_wtr_next	RW	0x00040505	32	3.3.124 <i>t_wtr_next</i> on page 3-89
0x24C	t_wtw_next	RW	0x10060404	32	3.3.125 <i>t_wtw_next</i> on page 3-89
0x254	t_xmpd_next	RW	0x000003FF	32	3.3.126 <i>t_xmpd_next</i> on page 3-89
0x258	t_ep_next	RW	0x00000002	32	3.3.127 <i>t_ep_next</i> on page 3-90
0x25C	t_xp_next	RW	0x00060002	32	3.3.128 <i>t_xp_next</i> on page 3-90
0x260	t_esr_next	RW	0x0000000E	32	3.3.129 <i>t_esr_next</i> on page 3-90
0x264	t_xsr_next	RW	0x05120100	32	3.3.130 <i>t_xsr_next</i> on page 3-91
0x268	t_esrck_next	RW	0x00000005	32	3.3.131 <i>t_esrck_next</i> on page 3-91
0x26C	t_ckxsr_next	RW	0x00000001	32	3.3.132 <i>t_ckxsr_next</i> on page 3-91
0x270	t_cmd_next	RW	0x00000000	32	3.3.133 <i>t_cmd_next</i> on page 3-92
0x274	t_parity_next	RW	0x00000900	32	3.3.134 <i>t_parity_next</i> on page 3-92
0x278	t_zqcs_next	RW	0x00000040	32	3.3.135 <i>t_zqcs_next</i> on page 3-92
0x27C	t_rw_odt_clr_next	RW	0x00000000	32	3.3.136 <i>t_rw_odt_clr_next</i> on page 3-92
0x300	t_rddata_en_next	RW	0x00000001	32	3.3.137 <i>t_rddata_en_next</i> on page 3-93
0x304	t_phyrdlat_next	RW	0x00000000	32	3.3.138 <i>t_phyrdlat_next</i> on page 3-93

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x308	t_phywrlat_next	RW	0x00000001	32	3.3.139 t_phywrlat_next on page 3-94
0x310	rdlvl_control_next	RW	0x00001080	32	3.3.140 rdlvl_control_next on page 3-94
0x314	rdlvl_mrs_next	RW	0x00000004	32	3.3.141 rdlvl_mrs_next on page 3-94
0x318	t_rdlvl_en_next	RW	0x00000000	32	3.3.142 t_rdlvl_en_next on page 3-95
0x31C	t_rdlvl_rr_next	RW	0x00000000	32	3.3.143 t_rdlvl_rr_next on page 3-95
0x320	wrlvl_control_next	RW	0x00101000	32	3.3.144 wrlvl_control_next on page 3-95
0x324	wrlvl_mrs_next	RW	0x00000086	32	3.3.145 wrlvl_mrs_next on page 3-96
0x328	t_wrlvl_en_next	RW	0x00000000	32	3.3.146 t_wrlvl_en_next on page 3-96
0x32C	t_wrlvl_ww_next	RW	0x00000000	32	3.3.147 t_wrlvl_ww_next on page 3-96
0x334	training_wrlvl_slice_status	RO	0x00000000	32	3.3.148 training_wrlvl_slice_status on page 3-97
0x338	training_rdlvl_slice_status	RO	0x00000000	32	3.3.149 training_rdlvl_slice_status on page 3-97
0x33C	training_rdlvl_gate_slice_status	RO	0x00000000	32	3.3.150 training_rdlvl_gate_slice_status on page 3-97
0x340	training_wdqlvl_slice_status	RO	0x00000000	32	3.3.151 training_wdqlvl_slice_status on page 3-97
0x344	training_wdqlvl_slice_result	RO	0x00000000	32	3.3.152 training_wdqlvl_slice_result on page 3-98
0x348	phy_power_control_next	RW	0x00000000	32	3.3.153 phy_power_control_next on page 3-98
0x34C	t_lpresp_next	RW	0x00000000	32	3.3.154 t_lpresp_next on page 3-98
0x350	phy_update_control_next	RW	0x2FE00000	32	3.3.155 phy_update_control_next on page 3-99
0x354	t_odth_next	RW	0x00000006	32	3.3.156 t_odth_next on page 3-99
0x358	odt_timing_next	RW	0x06000600	32	3.3.157 odt_timing_next on page 3-99
0x360	odt_wr_control_31_00_next	RW	0x08040201	32	3.3.158 odt_wr_control_31_00_next on page 3-100
0x364	odt_wr_control_63_32_next	RW	0x80402010	32	3.3.159 odt_wr_control_63_32_next on page 3-100
0x368	odt_rd_control_31_00_next	RW	0x00000000	32	3.3.160 odt_rd_control_31_00_next on page 3-100
0x36C	odt_rd_control_63_32_next	RW	0x00000000	32	3.3.161 odt_rd_control_63_32_next on page 3-100
0x370	temperature_readout	RO	0x00000000	32	3.3.162 temperature_readout on page 3-101
0x378	training_status	RO	0x00000000	32	3.3.163 training_status on page 3-101
0x37C	training_status_63_32	RO	0x00000000	32	3.3.164 training_status_63_32 on page 3-101
0x380	dq_map_control_15_00_next	RW	0x00000000	32	3.3.165 dq_map_control_15_00_next on page 3-102
0x384	dq_map_control_31_16_next	RW	0x00000000	32	3.3.166 dq_map_control_31_16_next on page 3-102
0x388	dq_map_control_47_32_next	RW	0x00000000	32	3.3.167 dq_map_control_47_32_next on page 3-102
0x38C	dq_map_control_63_48_next	RW	0x00000000	32	3.3.168 dq_map_control_63_48_next on page 3-103
0x390	dq_map_control_71_64_next	RW	0x00000000	32	3.3.169 dq_map_control_71_64_next on page 3-103
0x398	rank_status	RO	0x00000000	32	3.3.170 rank_status on page 3-103
0x39C	mode_change_status	RO	0x00000000	32	3.3.171 mode_change_status on page 3-104
0x3B0	odt_cp_control_31_00_next	RW	0x08040201	32	3.3.172 odt_cp_control_31_00_next on page 3-104

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x3B4	odt_cp_control_63_32_next	RW	0x80402010	32	<a href="#">3.3.173 odt_cp_control_63_32_next</a> on page 3-104
0x400	user_status	RO	0x00000000	32	<a href="#">3.3.174 user_status</a> on page 3-105
0x408	user_config0_next	RW	0x00000000	32	<a href="#">3.3.175 user_config0_next</a> on page 3-105
0x40C	user_config1_next	RW	0x00000000	32	<a href="#">3.3.176 user_config1_next</a> on page 3-105
0x410	user_config2	RW	0x00000000	32	<a href="#">3.3.177 user_config2</a> on page 3-106
0x414	user_config3	RW	0x00000000	32	<a href="#">3.3.178 user_config3</a> on page 3-106
0x500	interrupt_control	RW	0x00000000	32	<a href="#">3.3.179 interrupt_control</a> on page 3-106
0x508	interrupt_clr	WO	0x00000000	32	<a href="#">3.3.180 interrupt_clr</a> on page 3-106
0x510	interrupt_status	RO	0x00000000	32	<a href="#">3.3.181 interrupt_status</a> on page 3-107
0x538	failed_access_int_info_31_00	RO	0x00000000	32	<a href="#">3.3.182 failed_access_int_info_31_00</a> on page 3-107
0x53C	failed_access_int_info_63_32	RO	0x00000000	32	<a href="#">3.3.183 failed_access_int_info_63_32</a> on page 3-107
0x540	failed_prog_int_info_31_00	RO	0x00000000	32	<a href="#">3.3.184 failed_prog_int_info_31_00</a> on page 3-108
0x544	failed_prog_int_info_63_32	RO	0x00000000	32	<a href="#">3.3.185 failed_prog_int_info_63_32</a> on page 3-108
0x548	link_err_int_info_31_00	RO	0x00000000	32	<a href="#">3.3.186 link_err_int_info_31_00</a> on page 3-108
0x54C	link_err_int_info_63_32	RO	0x00000000	32	<a href="#">3.3.187 link_err_int_info_63_32</a> on page 3-109
0x550	arch_fsm_int_info_31_00	RO	0x00000000	32	<a href="#">3.3.188 arch_fsm_int_info_31_00</a> on page 3-109
0x554	arch_fsm_int_info_63_32	RO	0x00000000	32	<a href="#">3.3.189 arch_fsm_int_info_63_32</a> on page 3-109
0x610	t_db_train_resp_next	RW	0x00000000	32	<a href="#">3.3.190 t_db_train_resp_next</a> on page 3-109
0x614	t_lvl_disconnect_next	RW	0x0000000F	32	<a href="#">3.3.191 t_lvl_disconnect_next</a> on page 3-110
0x620	wdqlvl_control_next	RW	0x00000094	32	<a href="#">3.3.192 wdqlvl_control_next</a> on page 3-110
0x624	wdqlvl_vrefdq_train_mrs_next	RW	0x00000000	32	<a href="#">3.3.193 wdqlvl_vrefdq_train_mrs_next</a> on page 3-110
0x628	wdqlvl_address_31_00_next	RW	0x00000000	32	<a href="#">3.3.194 wdqlvl_address_31_00_next</a> on page 3-111
0x62C	wdqlvl_address_63_32_next	RW	0x00000000	32	<a href="#">3.3.195 wdqlvl_address_63_32_next</a> on page 3-111
0x630	t_wdqlvl_en_next	RW	0x00000000	32	<a href="#">3.3.196 t_wdqlvl_en_next</a> on page 3-111
0x634	t_wdqlvl_ww_next	RW	0x00000000	32	<a href="#">3.3.197 t_wdqlvl_ww_next</a> on page 3-112
0x638	t_wdqlvl_rw_next	RW	0x00000000	32	<a href="#">3.3.198 t_wdqlvl_rw_next</a> on page 3-112
0x63C	training_wdqlvl_slice_resp	RO	0x00000000	32	<a href="#">3.3.199 training_wdqlvl_slice_resp</a> on page 3-112
0x640	training_rdlvl_slice_resp	RO	0x00000000	32	<a href="#">3.3.200 training_rdlvl_slice_resp</a> on page 3-113
0x654	phymstr_control_next	RW	0x00000000	32	<a href="#">3.3.201 phymstr_control_next</a> on page 3-113
0x700	err0fr	RO	0x000009AA	32	<a href="#">3.3.202 err0fr</a> on page 3-113
0x708	err0ctrl0	RW	0x00000010	32	<a href="#">3.3.203 err0ctrl0</a> on page 3-114
0x70C	err0ctrl1	RW	0x000000C0	32	<a href="#">3.3.204 err0ctrl1</a> on page 3-114
0x710	err0status	RO	0x00000000	32	<a href="#">3.3.205 err0status</a> on page 3-114
0x740	err1fr	RO	0x000009AA	32	<a href="#">3.3.206 err1fr</a> on page 3-115
0x748	err1ctrl	RO	0x00000000	32	<a href="#">3.3.207 err1ctrl</a> on page 3-115

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x750	err1status	RW	0x00000000	32	<a href="#">3.3.208 err1status</a> on page 3-115
0x758	err1addr0	RW	0x00000000	32	<a href="#">3.3.209 err1addr0</a> on page 3-116
0x75C	err1addr1	RW	0x00000000	32	<a href="#">3.3.210 err1addr1</a> on page 3-116
0x760	err1misc0	RW	0x00000000	32	<a href="#">3.3.211 err1misc0</a> on page 3-116
0x764	err1misc1	RW	0x00000000	32	<a href="#">3.3.212 err1misc1</a> on page 3-117
0x768	err1misc2	RW	0x00000000	32	<a href="#">3.3.213 err1misc2</a> on page 3-117
0x76C	err1misc3	RW	0x00000000	32	<a href="#">3.3.214 err1misc3</a> on page 3-117
0x770	err1misc4	RW	0x00000000	32	<a href="#">3.3.215 err1misc4</a> on page 3-118
0x774	err1misc5	RW	0x00000000	32	<a href="#">3.3.216 err1misc5</a> on page 3-118
0x780	err2fr	RO	0x000009AA	32	<a href="#">3.3.217 err2fr</a> on page 3-118
0x788	err2ctrl	RO	0x00000000	32	<a href="#">3.3.218 err2ctrl</a> on page 3-118
0x790	err2status	RW	0x00000000	32	<a href="#">3.3.219 err2status</a> on page 3-119
0x798	err2addr0	RW	0x00000000	32	<a href="#">3.3.220 err2addr0</a> on page 3-119
0x79C	err2addr1	RW	0x00000000	32	<a href="#">3.3.221 err2addr1</a> on page 3-119
0x7A0	err2misc0	RW	0x00000000	32	<a href="#">3.3.222 err2misc0</a> on page 3-120
0x7A4	err2misc1	RW	0x00000000	32	<a href="#">3.3.223 err2misc1</a> on page 3-120
0x7A8	err2misc2	RW	0x00000000	32	<a href="#">3.3.224 err2misc2</a> on page 3-120
0x7AC	err2misc3	RW	0x00000000	32	<a href="#">3.3.225 err2misc3</a> on page 3-121
0x7B0	err2misc4	RW	0x00000000	32	<a href="#">3.3.226 err2misc4</a> on page 3-121
0x7B4	err2misc5	RW	0x00000000	32	<a href="#">3.3.227 err2misc5</a> on page 3-121
0x7C0	err3fr	RO	0x000009AA	32	<a href="#">3.3.228 err3fr</a> on page 3-122
0x7C8	err3ctrl	RO	0x00000000	32	<a href="#">3.3.229 err3ctrl</a> on page 3-122
0x7D0	err3status	RW	0x00000000	32	<a href="#">3.3.230 err3status</a> on page 3-122
0x7D8	err3addr0	RW	0x00000000	32	<a href="#">3.3.231 err3addr0</a> on page 3-122
0x7DC	err3addr1	RW	0x00000000	32	<a href="#">3.3.232 err3addr1</a> on page 3-123
0x800	err4fr	RO	0x000009AA	32	<a href="#">3.3.233 err4fr</a> on page 3-123
0x808	err4ctrl	RO	0x00000000	32	<a href="#">3.3.234 err4ctrl</a> on page 3-123
0x810	err4status	RW	0x00000000	32	<a href="#">3.3.235 err4status</a> on page 3-124
0x818	err4addr0	RW	0x00000000	32	<a href="#">3.3.236 err4addr0</a> on page 3-124
0x81C	err4addr1	RW	0x00000000	32	<a href="#">3.3.237 err4addr1</a> on page 3-124
0x820	err4misc0	RW	0x00000000	32	<a href="#">3.3.238 err4misc0</a> on page 3-125
0x824	err4misc1	RW	0x00000000	32	<a href="#">3.3.239 err4misc1</a> on page 3-125
0x828	err4misc2	RW	0x00000000	32	<a href="#">3.3.240 err4misc2</a> on page 3-125
0x840	err5fr	RO	0x000009AA	32	<a href="#">3.3.241 err5fr</a> on page 3-126
0x848	err5ctrl	RO	0x00000000	32	<a href="#">3.3.242 err5ctrl</a> on page 3-126



Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x850	err5status	RW	0x000000	32	<a href="#">3.3.243 err5status</a> on page 3-126
0x858	err5addr0	RW	0x00000000	32	<a href="#">3.3.244 err5addr0</a> on page 3-126
0x85C	err5addr1	RW	0x00000000	32	<a href="#">3.3.245 err5addr1</a> on page 3-127
0x860	err5misc0	RW	0x00000000	32	<a href="#">3.3.246 err5misc0</a> on page 3-127
0x864	err5misc1	RW	0x00000000	32	<a href="#">3.3.247 err5misc1</a> on page 3-127
0x868	err5misc2	RW	0x00000000	32	<a href="#">3.3.248 err5misc2</a> on page 3-128
0x880	err6fr	RO	0x000009AA	32	<a href="#">3.3.249 err6fr</a> on page 3-128
0x888	err6ctlr	RO	0x00000000	32	<a href="#">3.3.250 err6ctlr</a> on page 3-128
0x890	err6status	RW	0x000000	32	<a href="#">3.3.251 err6status</a> on page 3-129
0x898	err6addr0	RW	0x00000000	32	<a href="#">3.3.252 err6addr0</a> on page 3-129
0x89C	err6addr1	RW	0x00000000	32	<a href="#">3.3.253 err6addr1</a> on page 3-129
0x8A0	err6misc0	RW	0x00000000	32	<a href="#">3.3.254 err6misc0</a> on page 3-130
0x8A4	err6misc1	RW	0x00000000	32	<a href="#">3.3.255 err6misc1</a> on page 3-130
0x920	errgsr	RW	0x00000000	32	<a href="#">3.3.256 errgsr</a> on page 3-130
0xA00	pmu_snapshot_req	WO	0x00000000	32	<a href="#">3.3.257 pmu_snapshot_req</a> on page 3-130
0xA04	pmu_snapshot_ack	RO	0x00000000	32	<a href="#">3.3.258 pmu_snapshot_ack</a> on page 3-131
0xA08	pmu_overflow_status_clkdiv2	RW	0x00000000	32	<a href="#">3.3.259 pmu_overflow_status_clkdiv2</a> on page 3-131
0xA0C	pmu_overflow_status_clk	RW	0x00000000	32	<a href="#">3.3.260 pmu_overflow_status_clk</a> on page 3-131
0xA10	pmu_clkdiv2_counter_0_mask_31_00	RW	0x00000000	32	<a href="#">3.3.261 pmu_clkdiv2_counter_0_mask_31_00</a> on page 3-132
0xA14	pmu_clkdiv2_counter_0_mask_63_32	RW	0x00000000	32	<a href="#">3.3.262 pmu_clkdiv2_counter_0_mask_63_32</a> on page 3-132
0xA18	pmu_clkdiv2_counter_0_match_31_00	RW	0x00000000	32	<a href="#">3.3.263 pmu_clkdiv2_counter_0_match_31_00</a> on page 3-132
0xA1C	pmu_clkdiv2_counter_0_match_63_32	RW	0x00000000	32	<a href="#">3.3.264 pmu_clkdiv2_counter_0_match_63_32</a> on page 3-133
0xA20	pmu_clkdiv2_counter_0_control	RW	0x00000000	32	<a href="#">3.3.265 pmu_clkdiv2_counter_0_control</a> on page 3-133
0xA28	pmu_clkdiv2_counter_0_snapshot_value_31_00	RO	0x00000000	32	<a href="#">3.3.266 pmu_clkdiv2_counter_0_snapshot_value_31_00</a> on page 3-133
0xA30	pmu_clkdiv2_counter_0_value_31_00	RW	0x00000000	32	<a href="#">3.3.267 pmu_clkdiv2_counter_0_value_31_00</a> on page 3-133
0xA38	pmu_clkdiv2_counter_1_mask_31_00	RW	0x00000000	32	<a href="#">3.3.268 pmu_clkdiv2_counter_1_mask_31_00</a> on page 3-134
0xA3C	pmu_clkdiv2_counter_1_mask_63_32	RW	0x00000000	32	<a href="#">3.3.269 pmu_clkdiv2_counter_1_mask_63_32</a> on page 3-134
0xA40	pmu_clkdiv2_counter_1_match_31_00	RW	0x00000000	32	<a href="#">3.3.270 pmu_clkdiv2_counter_1_match_31_00</a> on page 3-134

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0xA44	pmu_clkdiv2_counter_1_match_63_32	RW	0x00000000	32	3.3.271 <i>pmu_clkdiv2_counter_1_match_63_32</i> on page 3-135
0xA48	pmu_clkdiv2_counter_1_control	RW	0x00000000	32	3.3.272 <i>pmu_clkdiv2_counter_1_control</i> on page 3-135
0xA50	pmu_clkdiv2_counter_1_snapshot_value_31_00	RO	0x00000000	32	3.3.273 <i>pmu_clkdiv2_counter_1_snapshot_value_31_00</i> on page 3-135
0xA58	pmu_clkdiv2_counter_1_value_31_00	RW	0x00000000	32	3.3.274 <i>pmu_clkdiv2_counter_1_value_31_00</i> on page 3-136
0xA60	pmu_clkdiv2_counter_2_mask_31_00	RW	0x00000000	32	3.3.275 <i>pmu_clkdiv2_counter_2_mask_31_00</i> on page 3-136
0xA64	pmu_clkdiv2_counter_2_mask_63_32	RW	0x00000000	32	3.3.276 <i>pmu_clkdiv2_counter_2_mask_63_32</i> on page 3-136
0xA68	pmu_clkdiv2_counter_2_match_31_00	RW	0x00000000	32	3.3.277 <i>pmu_clkdiv2_counter_2_match_31_00</i> on page 3-136
0xA6C	pmu_clkdiv2_counter_2_match_63_32	RW	0x00000000	32	3.3.278 <i>pmu_clkdiv2_counter_2_match_63_32</i> on page 3-137
0xA70	pmu_clkdiv2_counter_2_control	RW	0x00000000	32	3.3.279 <i>pmu_clkdiv2_counter_2_control</i> on page 3-137
0xA78	pmu_clkdiv2_counter_2_snapshot_value_31_00	RO	0x00000000	32	3.3.280 <i>pmu_clkdiv2_counter_2_snapshot_value_31_00</i> on page 3-137
0xA80	pmu_clkdiv2_counter_2_value_31_00	RW	0x00000000	32	3.3.281 <i>pmu_clkdiv2_counter_2_value_31_00</i> on page 3-138
0xA88	pmu_clkdiv2_counter_3_mask_31_00	RW	0x00000000	32	3.3.282 <i>pmu_clkdiv2_counter_3_mask_31_00</i> on page 3-138
0xA8C	pmu_clkdiv2_counter_3_mask_63_32	RW	0x00000000	32	3.3.283 <i>pmu_clkdiv2_counter_3_mask_63_32</i> on page 3-138
0xA90	pmu_clkdiv2_counter_3_match_31_00	RW	0x00000000	32	3.3.284 <i>pmu_clkdiv2_counter_3_match_31_00</i> on page 3-139
0xA94	pmu_clkdiv2_counter_3_match_63_32	RW	0x00000000	32	3.3.285 <i>pmu_clkdiv2_counter_3_match_63_32</i> on page 3-139
0xA98	pmu_clkdiv2_counter_3_control	RW	0x00000000	32	3.3.286 <i>pmu_clkdiv2_counter_3_control</i> on page 3-139
0xAA0	pmu_clkdiv2_counter_3_snapshot_value_31_00	RO	0x00000000	32	3.3.287 <i>pmu_clkdiv2_counter_3_snapshot_value_31_00</i> on page 3-139
0xAA8	pmu_clkdiv2_counter_3_value_31_00	RW	0x00000000	32	3.3.288 <i>pmu_clkdiv2_counter_3_value_31_00</i> on page 3-140
0xAB0	pmu_clkdiv2_counter_4_mask_31_00	RW	0x00000000	32	3.3.289 <i>pmu_clkdiv2_counter_4_mask_31_00</i> on page 3-140
0xAB4	pmu_clkdiv2_counter_4_mask_63_32	RW	0x00000000	32	3.3.290 <i>pmu_clkdiv2_counter_4_mask_63_32</i> on page 3-140
0xAB8	pmu_clkdiv2_counter_4_match_31_00	RW	0x00000000	32	3.3.291 <i>pmu_clkdiv2_counter_4_match_31_00</i> on page 3-141



Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0xABC	pmu_clkdiv2_counter_4_match_63_32	RW	0x00000000	32	3.3.292 <i>pmu_clkdiv2_counter_4_match_63_32</i> on page 3-141
0xAC0	pmu_clkdiv2_counter_4_control	RW	0x00000000	32	3.3.293 <i>pmu_clkdiv2_counter_4_control</i> on page 3-141
0xAC8	pmu_clkdiv2_counter_4_snapshot_value_31_00	RO	0x00000000	32	3.3.294 <i>pmu_clkdiv2_counter_4_snapshot_value_31_00</i> on page 3-142
0xAD0	pmu_clkdiv2_counter_4_value_31_00	RW	0x00000000	32	3.3.295 <i>pmu_clkdiv2_counter_4_value_31_00</i> on page 3-142
0xAD8	pmu_clkdiv2_counter_5_mask_31_00	RW	0x00000000	32	3.3.296 <i>pmu_clkdiv2_counter_5_mask_31_00</i> on page 3-142
0xADC	pmu_clkdiv2_counter_5_mask_63_32	RW	0x00000000	32	3.3.297 <i>pmu_clkdiv2_counter_5_mask_63_32</i> on page 3-142
0xAE0	pmu_clkdiv2_counter_5_match_31_00	RW	0x00000000	32	3.3.298 <i>pmu_clkdiv2_counter_5_match_31_00</i> on page 3-143
0xAE4	pmu_clkdiv2_counter_5_match_63_32	RW	0x00000000	32	3.3.299 <i>pmu_clkdiv2_counter_5_match_63_32</i> on page 3-143
0xAE8	pmu_clkdiv2_counter_5_control	RW	0x00000000	32	3.3.300 <i>pmu_clkdiv2_counter_5_control</i> on page 3-143
0xAF0	pmu_clkdiv2_counter_5_snapshot_value_31_00	RO	0x00000000	32	3.3.301 <i>pmu_clkdiv2_counter_5_snapshot_value_31_00</i> on page 3-144
0xAF8	pmu_clkdiv2_counter_5_value_31_00	RW	0x00000000	32	3.3.302 <i>pmu_clkdiv2_counter_5_value_31_00</i> on page 3-144
0xB00	pmu_clkdiv2_counter_6_mask_31_00	RW	0x00000000	32	3.3.303 <i>pmu_clkdiv2_counter_6_mask_31_00</i> on page 3-144
0xB04	pmu_clkdiv2_counter_6_mask_63_32	RW	0x00000000	32	3.3.304 <i>pmu_clkdiv2_counter_6_mask_63_32</i> on page 3-145
0xB08	pmu_clkdiv2_counter_6_match_31_00	RW	0x00000000	32	3.3.305 <i>pmu_clkdiv2_counter_6_match_31_00</i> on page 3-145
0xB0C	pmu_clkdiv2_counter_6_match_63_32	RW	0x00000000	32	3.3.306 <i>pmu_clkdiv2_counter_6_match_63_32</i> on page 3-145
0xB10	pmu_clkdiv2_counter_6_control	RW	0x00000000	32	3.3.307 <i>pmu_clkdiv2_counter_6_control</i> on page 3-145
0xB18	pmu_clkdiv2_counter_6_snapshot_value_31_00	RO	0x00000000	32	3.3.308 <i>pmu_clkdiv2_counter_6_snapshot_value_31_00</i> on page 3-146
0xB20	pmu_clkdiv2_counter_6_value_31_00	RW	0x00000000	32	3.3.309 <i>pmu_clkdiv2_counter_6_value_31_00</i> on page 3-146
0xB28	pmu_clkdiv2_counter_7_mask_31_00	RW	0x00000000	32	3.3.310 <i>pmu_clkdiv2_counter_7_mask_31_00</i> on page 3-146
0xB2C	pmu_clkdiv2_counter_7_mask_63_32	RW	0x00000000	32	3.3.311 <i>pmu_clkdiv2_counter_7_mask_63_32</i> on page 3-147
0xB30	pmu_clkdiv2_counter_7_match_31_00	RW	0x00000000	32	3.3.312 <i>pmu_clkdiv2_counter_7_match_31_00</i> on page 3-147

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0xB34	pmu_clkdiv2_counter_7_match_63_32	RW	0x00000000	32	3.3.313 <i>pmu_clkdiv2_counter_7_match_63_32</i> on page 3-147
0xB38	pmu_clkdiv2_counter_7_control	RW	0x00000000	32	3.3.314 <i>pmu_clkdiv2_counter_7_control</i> on page 3-148
0xB40	pmu_clkdiv2_counter_7_snapshot_value_31_00	RO	0x00000000	32	3.3.315 <i>pmu_clkdiv2_counter_7_snapshot_value_31_00</i> on page 3-148
0xB48	pmu_clkdiv2_counter_7_value_31_00	RW	0x00000000	32	3.3.316 <i>pmu_clkdiv2_counter_7_value_31_00</i> on page 3-148
0xB50	pmu_clk_counter_0_mask_31_00	RW	0x00000000	32	3.3.317 <i>pmu_clk_counter_0_mask_31_00</i> on page 3-148
0xB54	pmu_clk_counter_0_mask_63_32	RW	0x00000000	32	3.3.318 <i>pmu_clk_counter_0_mask_63_32</i> on page 3-149
0xB58	pmu_clk_counter_0_match_31_00	RW	0x00000000	32	3.3.319 <i>pmu_clk_counter_0_match_31_00</i> on page 3-149
0xB5C	pmu_clk_counter_0_match_63_32	RW	0x00000000	32	3.3.320 <i>pmu_clk_counter_0_match_63_32</i> on page 3-149
0xB60	pmu_clk_counter_0_control	RW	0x00000000	32	3.3.321 <i>pmu_clk_counter_0_control</i> on page 3-150
0xB68	pmu_clk_counter_0_snapshot_value_31_00	RO	0x00000000	32	3.3.322 <i>pmu_clk_counter_0_snapshot_value_31_00</i> on page 3-150
0xB70	pmu_clk_counter_0_value_31_00	RW	0x00000000	32	3.3.323 <i>pmu_clk_counter_0_value_31_00</i> on page 3-150
0xB78	pmu_clk_counter_1_mask_31_00	RW	0x00000000	32	3.3.324 <i>pmu_clk_counter_1_mask_31_00</i> on page 3-151
0xB7C	pmu_clk_counter_1_mask_63_32	RW	0x00000000	32	3.3.325 <i>pmu_clk_counter_1_mask_63_32</i> on page 3-151
0xB80	pmu_clk_counter_1_match_31_00	RW	0x00000000	32	3.3.326 <i>pmu_clk_counter_1_match_31_00</i> on page 3-151
0xB84	pmu_clk_counter_1_match_63_32	RW	0x00000000	32	3.3.327 <i>pmu_clk_counter_1_match_63_32</i> on page 3-151
0xB88	pmu_clk_counter_1_control	RW	0x00000000	32	3.3.328 <i>pmu_clk_counter_1_control</i> on page 3-152
0xB90	pmu_clk_counter_1_snapshot_value_31_00	RO	0x00000000	32	3.3.329 <i>pmu_clk_counter_1_snapshot_value_31_00</i> on page 3-152
0xB98	pmu_clk_counter_1_value_31_00	RW	0x00000000	32	3.3.330 <i>pmu_clk_counter_1_value_31_00</i> on page 3-152
0xE00	integ_cfg	RW	0x00000000	32	3.3.331 <i>integ_cfg</i> on page 3-153
0xE08	integ_outputs	WO	0x00000000	32	3.3.332 <i>integ_outputs</i> on page 3-153
0x1010	address_control_now	RO	0x00030202	32	3.3.333 <i>address_control_now</i> on page 3-153
0x1014	decode_control_now	RO	0x001A3000	32	3.3.334 <i>decode_control_now</i> on page 3-154

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x101 C	address_map_now	RO	0x00000000	32	<a href="#">3.3.335 address_map_now</a> on page 3-154
0x102 0	low_power_control_now	RO	0x00000020	32	<a href="#">3.3.336 low_power_control_now</a> on page 3-154
0x102 8	turnaround_control_now	RO	0x0F0F0F0F	32	<a href="#">3.3.337 turnaround_control_now</a> on page 3-155
0x102 C	hit_turnaround_control_now	RO	0x08909FBF	32	<a href="#">3.3.338 hit_turnaround_control_now</a> on page 3-155
0x103 0	qos_class_control_now	RO	0x0000FC8	32	<a href="#">3.3.339 qos_class_control_now</a> on page 3-155
0x103 4	escalation_control_now	RO	0x00080F03	32	<a href="#">3.3.340 escalation_control_now</a> on page 3-156
0x103 8	qv_control_31_00_now	RO	0x76543210	32	<a href="#">3.3.341 qv_control_31_00_now</a> on page 3-156
0x103 C	qv_control_63_32_now	RO	0xFEDCBA98	32	<a href="#">3.3.342 qv_control_63_32_now</a> on page 3-156
0x104 0	rt_control_31_00_now	RO	0x00000000	32	<a href="#">3.3.343 rt_control_31_00_now</a> on page 3-157
0x104 4	rt_control_63_32_now	RO	0x00000000	32	<a href="#">3.3.344 rt_control_63_32_now</a> on page 3-157
0x104 8	timeout_control_now	RO	0x00000001	32	<a href="#">3.3.345 timeout_control_now</a> on page 3-157
0x104 C	credit_control_now	RO	0x0000F03	32	<a href="#">3.3.346 credit_control_now</a> on page 3-158
0x105 0	write_priority_control_31_00_now	RO	0x00000000	32	<a href="#">3.3.347 write_priority_control_31_00_now</a> on page 3-158
0x105 4	write_priority_control_63_32_now	RO	0x00000000	32	<a href="#">3.3.348 write_priority_control_63_32_now</a> on page 3-158
0x105 8	queue_threshold_control_31_00_now	RO	0x00000008	32	<a href="#">3.3.349 queue_threshold_control_31_00_now</a> on page 3-159
0x105 C	queue_threshold_control_63_32_now	RO	0x00000000	32	<a href="#">3.3.350 queue_threshold_control_63_32_now</a> on page 3-159
0x106 0	address_shutter_31_00_now	RO	0x00000000	32	<a href="#">3.3.351 address_shutter_31_00_now</a> on page 3-159
0x106 4	address_shutter_63_32_now	RO	0x00000000	32	<a href="#">3.3.352 address_shutter_63_32_now</a> on page 3-160
0x106 8	address_shutter_95_64_now	RO	0x00000000	32	<a href="#">3.3.353 address_shutter_95_64_now</a> on page 3-160
0x106 C	address_shutter_127_96_now	RO	0x00000000	32	<a href="#">3.3.354 address_shutter_127_96_now</a> on page 3-160
0x107 0	address_shutter_159_128_now	RO	0x00000000	32	<a href="#">3.3.355 address_shutter_159_128_now</a> on page 3-161

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1074	address_shutter_191_160_now	RO	0x00000000	32	3.3.356 <i>address_shutter_191_160_now</i> on page 3-161
0x1078	memory_address_max_31_00_now	RO	0x00000010	32	3.3.357 <i>memory_address_max_31_00_now</i> on page 3-161
0x107C	memory_address_max_47_32_now	RO	0x00000000	32	3.3.358 <i>memory_address_max_47_32_now</i> on page 3-162
0x1080	access_address_min0_31_00_now	RO	0x00000000	32	3.3.359 <i>access_address_min0_31_00_now</i> on page 3-162
0x1084	access_address_min0_47_32_now	RO	0x00000000	32	3.3.360 <i>access_address_min0_47_32_now</i> on page 3-162
0x1088	access_address_max0_31_00_now	RO	0x00000000	32	3.3.361 <i>access_address_max0_31_00_now</i> on page 3-163
0x108C	access_address_max0_47_32_now	RO	0x00000000	32	3.3.362 <i>access_address_max0_47_32_now</i> on page 3-163
0x1090	access_address_min1_31_00_now	RO	0x00000000	32	3.3.363 <i>access_address_min1_31_00_now</i> on page 3-163
0x1094	access_address_min1_47_32_now	RO	0x00000000	32	3.3.364 <i>access_address_min1_47_32_now</i> on page 3-164
0x1098	access_address_max1_31_00_now	RO	0x00000000	32	3.3.365 <i>access_address_max1_31_00_now</i> on page 3-164
0x109C	access_address_max1_47_32_now	RO	0x00000000	32	3.3.366 <i>access_address_max1_47_32_now</i> on page 3-164
0x10A0	access_address_min2_31_00_now	RO	0x00000000	32	3.3.367 <i>access_address_min2_31_00_now</i> on page 3-165
0x10A4	access_address_min2_47_32_now	RO	0x00000000	32	3.3.368 <i>access_address_min2_47_32_now</i> on page 3-165
0x10A8	access_address_max2_31_00_now	RO	0x00000000	32	3.3.369 <i>access_address_max2_31_00_now</i> on page 3-165
0x10AC	access_address_max2_47_32_now	RO	0x00000000	32	3.3.370 <i>access_address_max2_47_32_now</i> on page 3-166
0x10B0	access_address_min3_31_00_now	RO	0x00000000	32	3.3.371 <i>access_address_min3_31_00_now</i> on page 3-166
0x10B4	access_address_min3_47_32_now	RO	0x00000000	32	3.3.372 <i>access_address_min3_47_32_now</i> on page 3-166
0x10B8	access_address_max3_31_00_now	RO	0x00000000	32	3.3.373 <i>access_address_max3_31_00_now</i> on page 3-167
0x10BC	access_address_max3_47_32_now	RO	0x00000000	32	3.3.374 <i>access_address_max3_47_32_now</i> on page 3-167
0x10C0	access_address_min4_31_00_now	RO	0x00000000	32	3.3.375 <i>access_address_min4_31_00_now</i> on page 3-167
0x10C4	access_address_min4_47_32_now	RO	0x00000000	32	3.3.376 <i>access_address_min4_47_32_now</i> on page 3-168

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x10C8	access_address_max4_31_00_now	RO	0x00000000	32	3.3.377 <i>access_address_max4_31_00_now</i> on page 3-168
0x10CC	access_address_max4_47_32_now	RO	0x00000000	32	3.3.378 <i>access_address_max4_47_32_now</i> on page 3-168
0x10D0	access_address_min5_31_00_now	RO	0x00000000	32	3.3.379 <i>access_address_min5_31_00_now</i> on page 3-169
0x10D4	access_address_min5_47_32_now	RO	0x00000000	32	3.3.380 <i>access_address_min5_47_32_now</i> on page 3-169
0x10D8	access_address_max5_31_00_now	RO	0x00000000	32	3.3.381 <i>access_address_max5_31_00_now</i> on page 3-169
0x10DC	access_address_max5_47_32_now	RO	0x00000000	32	3.3.382 <i>access_address_max5_47_32_now</i> on page 3-170
0x10E0	access_address_min6_31_00_now	RO	0x00000000	32	3.3.383 <i>access_address_min6_31_00_now</i> on page 3-170
0x10E4	access_address_min6_47_32_now	RO	0x00000000	32	3.3.384 <i>access_address_min6_47_32_now</i> on page 3-170
0x10E8	access_address_max6_31_00_now	RO	0x00000000	32	3.3.385 <i>access_address_max6_31_00_now</i> on page 3-171
0x10EC	access_address_max6_47_32_now	RO	0x00000000	32	3.3.386 <i>access_address_max6_47_32_now</i> on page 3-171
0x10F0	access_address_min7_31_00_now	RO	0x00000000	32	3.3.387 <i>access_address_min7_31_00_now</i> on page 3-171
0x10F4	access_address_min7_47_32_now	RO	0x00000000	32	3.3.388 <i>access_address_min7_47_32_now</i> on page 3-172
0x10F8	access_address_max7_31_00_now	RO	0x00000000	32	3.3.389 <i>access_address_max7_31_00_now</i> on page 3-172
0x10FC	access_address_max7_47_32_now	RO	0x00000000	32	3.3.390 <i>access_address_max7_47_32_now</i> on page 3-172
0x1110	dc_i_replay_type_now	RO	0x00000002	32	3.3.391 <i>dc_i_replay_type_now</i> on page 3-173
0x1114	direct_control_now	RO	0x0003FFFF	32	3.3.392 <i>direct_control_now</i> on page 3-173
0x1120	refresh_control_now	RO	0x00000000	32	3.3.393 <i>refresh_control_now</i> on page 3-173
0x1128	memory_type_now	RO	0x00000101	32	3.3.394 <i>memory_type_now</i> on page 3-173
0x1170	scrub_control0_now	RO	0x0FFFFFF0	32	3.3.395 <i>scrub_control0_now</i> on page 3-174
0x1174	scrub_address_min0_now	RO	0x00000000	32	3.3.396 <i>scrub_address_min0_now</i> on page 3-174
0x1178	scrub_address_max0_now	RO	0x00000000	32	3.3.397 <i>scrub_address_max0_now</i> on page 3-174

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x1180	scrub_control1_now	RO	0x0FFFFFF0	32	<a href="#">3.3.398 scrub_control1_now</a> on page 3-175
0x1184	scrub_address_min1_now	RO	0x00000000	32	<a href="#">3.3.399 scrub_address_min1_now</a> on page 3-175
0x1188	scrub_address_max1_now	RO	0x00000000	32	<a href="#">3.3.400 scrub_address_max1_now</a> on page 3-175
0x11A0	cs_remap_control_31_00_now	RO	0x00020001	32	<a href="#">3.3.401 cs_remap_control_31_00_now</a> on page 3-176
0x11A4	cs_remap_control_63_32_now	RO	0x00080004	32	<a href="#">3.3.402 cs_remap_control_63_32_now</a> on page 3-176
0x11A8	cs_remap_control_95_64_now	RO	0x00200010	32	<a href="#">3.3.403 cs_remap_control_95_64_now</a> on page 3-176
0x11AC	cs_remap_control_127_96_now	RO	0x00800040	32	<a href="#">3.3.404 cs_remap_control_127_96_now</a> on page 3-177
0x11B0	cid_remap_control_31_00_now	RO	0x20001000	32	<a href="#">3.3.405 cid_remap_control_31_00_now</a> on page 3-177
0x11B4	cid_remap_control_63_32_now	RO	0x00004000	32	<a href="#">3.3.406 cid_remap_control_63_32_now</a> on page 3-177
0x11C0	cke_remap_control_now	RO	0x76543210	32	<a href="#">3.3.407 cke_remap_control_now</a> on page 3-177
0x11C4	rst_remap_control_now	RO	0x76543210	32	<a href="#">3.3.408 rst_remap_control_now</a> on page 3-178
0x11C8	ck_remap_control_now	RO	0x76543210	32	<a href="#">3.3.409 ck_remap_control_now</a> on page 3-178
0x11D0	power_group_control_31_00_now	RO	0x00020001	32	<a href="#">3.3.410 power_group_control_31_00_now</a> on page 3-178
0x11D4	power_group_control_63_32_now	RO	0x00080004	32	<a href="#">3.3.411 power_group_control_63_32_now</a> on page 3-179
0x11D8	power_group_control_95_64_now	RO	0x00200010	32	<a href="#">3.3.412 power_group_control_95_64_now</a> on page 3-179
0x11DC	power_group_control_127_96_now	RO	0x00800040	32	<a href="#">3.3.413 power_group_control_127_96_now</a> on page 3-179
0x11F0	feature_control_now	RO	0x0AA00000	32	<a href="#">3.3.414 feature_control_now</a> on page 3-180
0x11F4	mux_control_now	RO	0x00000000	32	<a href="#">3.3.415 mux_control_now</a> on page 3-180
0x11F8	rank_remap_control_now	RO	0x76543210	32	<a href="#">3.3.416 rank_remap_control_now</a> on page 3-180
0x1200	t_refi_now	RO	0x00090100	32	<a href="#">3.3.417 t_refi_now</a> on page 3-181
0x1204	t_rfc_now	RO	0x00008C23	32	<a href="#">3.3.418 t_rfc_now</a> on page 3-181

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x1208	t_mrr_now	RO	0x00000002	32	<a href="#">3.3.419 t_mrr_now on page 3-181</a>
0x120C	t_mrw_now	RO	0x0000000C	32	<a href="#">3.3.420 t_mrw_now on page 3-182</a>
0x1218	t_rcd_now	RO	0x00000005	32	<a href="#">3.3.421 t_rcd_now on page 3-182</a>
0x121C	t_ras_now	RO	0x0000000E	32	<a href="#">3.3.422 t_ras_now on page 3-182</a>
0x1220	t_rp_now	RO	0x00000005	32	<a href="#">3.3.423 t_rp_now on page 3-183</a>
0x1224	t_rpall_now	RO	0x00000005	32	<a href="#">3.3.424 t_rpall_now on page 3-183</a>
0x1228	t_rrd_now	RO	0x04000404	32	<a href="#">3.3.425 t_rrd_now on page 3-183</a>
0x122C	t_act_window_now	RO	0x03561414	32	<a href="#">3.3.426 t_act_window_now on page 3-184</a>
0x1234	t_rtr_now	RO	0x10060404	32	<a href="#">3.3.427 t_rtr_now on page 3-184</a>
0x1238	t_rtw_now	RO	0x00060606	32	<a href="#">3.3.428 t_rtw_now on page 3-184</a>
0x123C	t_rtp_now	RO	0x00000004	32	<a href="#">3.3.429 t_rtp_now on page 3-185</a>
0x1244	t_wr_now	RO	0x00000005	32	<a href="#">3.3.430 t_wr_now on page 3-185</a>
0x1248	t_wtr_now	RO	0x00040505	32	<a href="#">3.3.431 t_wtr_now on page 3-185</a>
0x124C	t_wtw_now	RO	0x10060404	32	<a href="#">3.3.432 t_wtw_now on page 3-186</a>
0x1254	t_xmpd_now	RO	0x000003FF	32	<a href="#">3.3.433 t_xmpd_now on page 3-186</a>
0x1258	t_ep_now	RO	0x00000002	32	<a href="#">3.3.434 t_ep_now on page 3-186</a>
0x125C	t_xp_now	RO	0x00060002	32	<a href="#">3.3.435 t_xp_now on page 3-187</a> >
0x1260	t_esr_now	RO	0x0000000E	32	<a href="#">3.3.436 t_esr_now on page 3-187</a>
0x1264	t_xsr_now	RO	0x05120100	32	<a href="#">3.3.437 t_xsr_now on page 3-187</a>
0x1268	t_esrck_now	RO	0x00000005	32	<a href="#">3.3.438 t_esrck_now on page 3-188</a>
0x126C	t_ckxsr_now	RO	0x00000001	32	<a href="#">3.3.439 t_ckxsr_now on page 3-188</a>



**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x127 0	t_cmd_now	RO	0x00000000	32	3.3.440 t_cmd_now on page 3-188
0x127 4	t_parity_now	RO	0x00000900	32	3.3.441 t_parity_now on page 3-189
0x127 8	t_zqcs_now	RO	0x00000040	32	3.3.442 t_zqcs_now on page 3-189
0x127 C	t_rw_odt_clr_now	RO	0x00000000	32	3.3.443 t_rw_odt_clr_now on page 3-189
0x130 0	t_rddata_en_now	RO	0x00000001	32	3.3.444 t_rddata_en_now on page 3-190
0x130 4	t_phyrdlat_now	RO	0x00000000	32	3.3.445 t_phyrdlat_now on page 3-190
0x130 8	t_phywrlat_now	RO	0x00000001	32	3.3.446 t_phywrlat_now on page 3-190
0x131 0	rdlvl_control_now	RO	0x00001080	32	3.3.447 rdlvl_control_now on page 3-191
0x131 4	rdlvl_mrs_now	RO	0x00000004	32	3.3.448 rdlvl_mrs_now on page 3-191
0x131 8	t_rdlvl_en_now	RO	0x00000000	32	3.3.449 t_rdlvl_en_now on page 3-191
0x131 C	t_rdlvl_rr_now	RO	0x00000000	32	3.3.450 t_rdlvl_rr_now on page 3-192
0x132 0	wrlvl_control_now	RO	0x00101000	32	3.3.451 wrlvl_control_now on page 3-192
0x132 4	wrlvl_mrs_now	RO	0x00000086	32	3.3.452 wrlvl_mrs_now on page 3-192
0x132 8	t_wrlvl_en_now	RO	0x00000000	32	3.3.453 t_wrlvl_en_now on page 3-193
0x132 C	t_wrlvl_ww_now	RO	0x00000000	32	3.3.454 t_wrlvl_ww_now on page 3-193
0x134 8	phy_power_control_now	RO	0x00000000	32	3.3.455 phy_power_control_now on page 3-193
0x134 C	t_lpresp_now	RO	0x00000000	32	3.3.456 t_lpresp_now on page 3-194
0x135 0	phy_update_control_now	RO	0x2FE00000	32	3.3.457 phy_update_control_now on page 3-194
0x135 4	t_odth_now	RO	0x00000006	32	3.3.458 t_odth_now on page 3-194
0x135 8	odt_timing_now	RO	0x06000600	32	3.3.459 odt_timing_now on page 3-195
0x136 0	odt_wr_control_31_00_now	RO	0x08040201	32	3.3.460 odt_wr_control_31_00_now on page 3-195



**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x1364	odt_wr_control_63_32_now	RO	0x80402010	32	3.3.461 odt_wr_control_63_32_now on page 3-195
0x1368	odt_rd_control_31_00_now	RO	0x00000000	32	3.3.462 odt_rd_control_31_00_now on page 3-196
0x136C	odt_rd_control_63_32_now	RO	0x00000000	32	3.3.463 odt_rd_control_63_32_now on page 3-196
0x1380	dq_map_control_15_00_now	RO	0x00000000	32	3.3.464 dq_map_control_15_00_now on page 3-196
0x1384	dq_map_control_31_16_now	RO	0x00000000	32	3.3.465 dq_map_control_31_16_now on page 3-197
0x1388	dq_map_control_47_32_now	RO	0x00000000	32	3.3.466 dq_map_control_47_32_now on page 3-197
0x138C	dq_map_control_63_48_now	RO	0x00000000	32	3.3.467 dq_map_control_63_48_now on page 3-197
0x1390	dq_map_control_71_64_now	RO	0x00000000	32	3.3.468 dq_map_control_71_64_now on page 3-198
0x13B0	odt_cp_control_31_00_now	RO	0x08040201	32	3.3.469 odt_cp_control_31_00_now on page 3-198
0x13B4	odt_cp_control_63_32_now	RO	0x80402010	32	3.3.470 odt_cp_control_63_32_now on page 3-198
0x1408	user_config0_now	RO	0x00000000	32	3.3.471 user_config0_now on page 3-199
0x140C	user_config1_now	RO	0x00000000	32	3.3.472 user_config1_now on page 3-199
0x1610	t_db_train_resp_now	RO	0x00000000	32	3.3.473 t_db_train_resp_now on page 3-199
0x1614	t_lvl_disconnect_now	RO	0x0000000F	32	3.3.474 t_lvl_disconnect_now on page 3-200
0x1620	wdqlvl_control_now	RO	0x00000094	32	3.3.475 wdqlvl_control_now on page 3-200
0x1624	wdqlvl_vrefdq_train_mrs_now	RO	0x00000000	32	3.3.476 wdqlvl_vrefdq_train_mrs_now on page 3-200
0x1628	wdqlvl_address_31_00_now	RO	0x00000000	32	3.3.477 wdqlvl_address_31_00_now on page 3-201
0x162C	wdqlvl_address_63_32_now	RO	0x00000000	32	3.3.478 wdqlvl_address_63_32_now on page 3-201
0x1630	t_wdqlvl_en_now	RO	0x00000000	32	3.3.479 t_wdqlvl_en_now on page 3-201
0x1634	t_wdqlvl_ww_now	RO	0x00000000	32	3.3.480 t_wdqlvl_ww_now on page 3-202
0x1638	t_wdqlvl_rw_now	RO	0x00000000	32	3.3.481 t_wdqlvl_rw_now on page 3-202

**Table 3-1 Register summary (continued)**

Offset	Name	Type	Reset	Width	Description
0x1654	phymstr_control_now	RO	0x00000000	32	<a href="#">3.3.482 phymstr_control_now on page 3-202</a>
0x1FD0	periph_id_4	RO	0x00000014	32	<a href="#">3.3.483 periph_id_4 on page 3-203</a>
0x1FE0	periph_id_0	RO	0x00000054	32	<a href="#">3.3.484 periph_id_0 on page 3-203</a>
0x1FE4	periph_id_1	RO	0x000000B4	32	<a href="#">3.3.485 periph_id_1 on page 3-203</a>
0x1FE8	periph_id_2	RO	0x0000000B	32	<a href="#">3.3.486 periph_id_2 on page 3-203</a>
0x1FEC	periph_id_3	RO	0x00000000	32	<a href="#">3.3.487 periph_id_3 on page 3-204</a>
0x1FF0	component_id_0	RO	0x0000000D	32	<a href="#">3.3.488 component_id_0 on page 3-204</a>
0x1FF4	component_id_1	RO	0x000000F0	32	<a href="#">3.3.489 component_id_1 on page 3-204</a>
0x1FF8	component_id_2	RO	0x00000005	32	<a href="#">3.3.490 component_id_2 on page 3-205</a>
0x1FFC	component_id_3	RO	0x000000B1	32	<a href="#">3.3.491 component_id_3 on page 3-205</a>

## 3.3 Register descriptions

This section describes the dmc620 registers.

[3.2 Register summary on page 3-31](#) provides cross references to individual registers.

### 3.3.1 memc\_status

Holds the architectural status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The memc\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x000
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.2 memc\_config

Holds the configuration data for the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The memc\_config register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x004
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.3 memc\_cmd

Used to change the architectural state of the DMC, or execute queued manager operations. Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The memc\_cmd register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x008
<b>Type</b>	Write-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.4 address\_control\_next

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x010
<b>Type</b>	Read-write
<b>Reset</b>	0x00030202
<b>Width</b>	32

### 3.3.5 decode\_control\_next

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, cid, bank, row, and the column address. Note: Order fields must be unique, ie. row\_order != bank\_order != rank\_order. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The decode\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x014
<b>Type</b>	Read-write
<b>Reset</b>	0x001A3000
<b>Width</b>	32

### 3.3.6 format\_control

Configures the memory burst access parameters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The format\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x018
<b>Type</b>	Read-write
<b>Reset</b>	0x12000113
<b>Width</b>	32

### 3.3.7 address\_map\_next

Configures the system address mapping options. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address\_map\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x01C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.8 low\_power\_control\_next

Configures the low-power features of the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The low\_power\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x020
<b>Type</b>	Read-write
<b>Reset</b>	0x00000020
<b>Width</b>	32

### 3.3.9 turnaround\_control\_next

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The turnaround\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x028
<b>Type</b>	Read-write
<b>Reset</b>	0x0F0F0F0F
<b>Width</b>	32

### 3.3.10 hit\_turnaround\_control\_next

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The hit\_turnaround\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x02C
<b>Type</b>	Read-write
<b>Reset</b>	0x08909FBF
<b>Width</b>	32

### 3.3.11 qos\_class\_control\_next

Configures the priority class for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qos\_class\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x030
<b>Type</b>	Read-write
<b>Reset</b>	0x00000FC8
<b>Width</b>	32

### 3.3.12 escalation\_control\_next

Configures the settings for escalating the priority of entries in the queue. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The escalation\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x034
<b>Type</b>	Read-write
<b>Reset</b>	0x00080F03
<b>Width</b>	32

### 3.3.13 qv\_control\_31\_00\_next

Configures the priority settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qv\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x038
<b>Type</b>	Read-write
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.14 **qv\_control\_63\_32\_next**

Configures the priority settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qv\_control\_63\_32\_next register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

<b>Offset</b>	0x03C
<b>Type</b>	Read-write
<b>Reset</b>	0xFEDCBA98
<b>Width</b>	32

### 3.3.15 **rt\_control\_31\_00\_next**

Configures the timeout settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rt\_control\_31\_00\_next register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

<b>Offset</b>	0x040
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.16 **rt\_control\_63\_32\_next**

Configures the timeout settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rt\_control\_63\_32\_next register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

<b>Offset</b>	0x044
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.17 timeout\_control\_next

Configures the prescaler applied to timeout values. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The timeout\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x048
<b>Type</b>	Read-write
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.18 credit\_control\_next

Configures the settings for preventing starvation of CHI protocol retries. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The credit\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x04C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000F03
<b>Width</b>	32

### 3.3.19 write\_priority\_control\_31\_00\_next

Configures the priority settings for write requests within the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The write\_priority\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x050
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.20 write\_priority\_control\_63\_32\_next

Configures the priority settings for write requests within the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The write\_priority\_control\_63\_32\_next register characteristics are:



#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x054
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.21 queue\_threshold\_control\_31\_00\_next

Configures the threshold settings for requests in the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The queue\_threshold\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x058
<b>Type</b>	Read-write
<b>Reset</b>	0x00000008
<b>Width</b>	32

### 3.3.22 queue\_threshold\_control\_63\_32\_next

Configures the threshold settings for requests in the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The queue\_threshold\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x05C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.23 address\_shutter\_31\_00\_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address\_shutter\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x060
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.24 address\_shutter\_63\_32\_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The address\_shutter\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x064
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.25 address\_shutter\_95\_64\_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The address\_shutter\_95\_64\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x068
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.26 address\_shutter\_127\_96\_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The address\_shutter\_127\_96\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x06C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.27 address\_shutter\_159\_128\_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The address\_shutter\_159\_128\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x070
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.28 address\_shutter\_191\_160\_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The address\_shutter\_191\_160\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x074
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.29 memory\_address\_max\_31\_00\_next

Configures the address space control for the DMC default region. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The memory\_address\_max\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x078
<b>Type</b>	Read-write
<b>Reset</b>	0x00000010
<b>Width</b>	32

### 3.3.30 memory\_address\_max\_47\_32\_next

Configures the address space control for the DMC default region. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The memory\_address\_max\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x07C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.31 access\_address\_min0\_31\_00\_next

Configures the address space control for address region 0. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min0\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x080
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.32 access\_address\_min0\_47\_32\_next

Configures the address space control for address region 0. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min0\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x084
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.33 access\_address\_max0\_31\_00\_next

Configures the address space control for address region 0. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max0\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x088
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.34 access\_address\_max0\_47\_32\_next

Configures the address space control for address region 0. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max0\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x08C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.35 access\_address\_min1\_31\_00\_next

Configures the address space control for address region 1. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min1\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x090
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.36 access\_address\_min1\_47\_32\_next

Configures the address space control for address region 1. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min1\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x094
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.37 access\_address\_max1\_31\_00\_next

Configures the address space control for address region 1. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max1\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x098
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.38 access\_address\_max1\_47\_32\_next

Configures the address space control for address region 1. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max1\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x09C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.39 access\_address\_min2\_31\_00\_next

Configures the address space control for address region 2. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min2\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0A0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.40 access\_address\_min2\_47\_32\_next

Configures the address space control for address region 2. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min2\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0A4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.41 access\_address\_max2\_31\_00\_next

Configures the address space control for address region 2. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max2\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0A8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.42 access\_address\_max2\_47\_32\_next

Configures the address space control for address region 2. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max2\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0AC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.43 access\_address\_min3\_31\_00\_next

Configures the address space control for address region 3. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min3\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0B0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

#### 3.3.44 access\_address\_min3\_47\_32\_next

Configures the address space control for address region 3. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min3\_47\_32\_next register characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

There is only one DMC configuration.

##### Attributes

<b>Offset</b>	0x0B4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

#### 3.3.45 access\_address\_max3\_31\_00\_next

Configures the address space control for address region 3. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max3\_31\_00\_next register characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

There is only one DMC configuration.

##### Attributes

<b>Offset</b>	0x0B8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

#### 3.3.46 access\_address\_max3\_47\_32\_next

Configures the address space control for address region 3. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max3\_47\_32\_next register characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

There is only one DMC configuration.

##### Attributes

<b>Offset</b>	0x0BC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32



### 3.3.47 access\_address\_min4\_31\_00\_next

Configures the address space control for address region 4. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min4\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0C0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.48 access\_address\_min4\_47\_32\_next

Configures the address space control for address region 4. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min4\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0C4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.49 access\_address\_max4\_31\_00\_next

Configures the address space control for address region 4. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max4\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0C8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.50 access\_address\_max4\_47\_32\_next

Configures the address space control for address region 4. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max4\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0CC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.51 access\_address\_min5\_31\_00\_next

Configures the address space control for address region 5. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min5\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0D0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.52 access\_address\_min5\_47\_32\_next

Configures the address space control for address region 5. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min5\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0D4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.53 access\_address\_max5\_31\_00\_next

Configures the address space control for address region 5. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max5\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0D8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.54 access\_address\_max5\_47\_32\_next

Configures the address space control for address region 5. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max5\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0DC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.55 access\_address\_min6\_31\_00\_next

Configures the address space control for address region 6. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min6\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0E0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.56 access\_address\_min6\_47\_32\_next

Configures the address space control for address region 6. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min6\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0E4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.57 access\_address\_max6\_31\_00\_next

Configures the address space control for address region 6. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max6\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0E8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.58 access\_address\_max6\_47\_32\_next

Configures the address space control for address region 6. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max6\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0EC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.59 access\_address\_min7\_31\_00\_next

Configures the address space control for address region 7. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min7\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0F0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.60 access\_address\_min7\_47\_32\_next

Configures the address space control for address region 7. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_min7\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0F4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.61 access\_address\_max7\_31\_00\_next

Configures the address space control for address region 7. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max7\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0F8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.62 access\_address\_max7\_47\_32\_next

Configures the address space control for the address region 7. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access\_address\_max7\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x0FC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.63 channel\_status

Holds the current status of the memory channel. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The channel\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x100
<b>Type</b>	Read-only
<b>Reset</b>	0x00000003
<b>Width</b>	32

### 3.3.64 channel\_status\_63\_32

Holds the current status of the memory channel. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The channel\_status\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x104
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.65 direct\_addr

Sets the direct command address field for direct commands. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

The direct\_addr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x108
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.66 direct\_cmd

Generates direct commands from the manager. Access restrictions: WO Cannot be read from. Can be written to when in CONFIG, PAUSED or READY states.

The direct\_cmd register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10C
<b>Type</b>	Write-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.67 dci\_replay\_type\_next

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dci\_replay\_type\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x110
<b>Type</b>	Read-write
<b>Reset</b>	0x00000002
<b>Width</b>	32

### 3.3.68 direct\_control\_next

Represents the training configuration of the DMC executed by a direct command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The direct\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x114
<b>Type</b>	Read-write
<b>Reset</b>	0x0003FFFF
<b>Width</b>	32

### 3.3.69 dci\_strb

Configures the write data strobe values used during direct\_cmd WRITE operations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

The dci\_strb register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x118
<b>Type</b>	Read-write
<b>Reset</b>	0x0000000F
<b>Width</b>	32

### 3.3.70 dci\_data

Reading from this register location returns read data received a result of a READ command. Writing to this register location sets the data to be used for direct\_cmd WRITE commands. You must read or write

once for each 32-bit data word of a DRAM burst. Access restrictions: RW Can be read from when in CONFIG, PAUSED or READY states. Can be written to when in CONFIG, PAUSED or READY states.

The dci\_data register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x11C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.71 refresh\_control\_next

Configures the type of refresh commands issued by the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The refresh\_control\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x120
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.72 memory\_type\_next

Configures the DMC for the attached memory type. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The memory\_type\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x128
<b>Type</b>	Read-write
<b>Reset</b>	0x00000101
<b>Width</b>	32

### 3.3.73 feature\_config

Control register for DMC features. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The feature\_config register characteristics are:

**Usage constraints**

There are no usage constraints.



#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x130
<b>Type</b>	Read-write
<b>Reset</b>	0x000018E0
<b>Width</b>	32

### 3.3.74 nibble\_failed\_031\_000

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble\_failed\_031\_000 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x138
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.75 nibble\_failed\_063\_032

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble\_failed\_063\_032 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x13C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.76 nibble\_failed\_095\_064

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble\_failed\_095\_064 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x140
<b>Type</b>	Read-write

**Reset** 0x00000000  
**Width** 32

### 3.3.77 nibble\_failed\_127\_096

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble\_failed\_127\_096 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x144  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.78 queue\_allocate\_control\_031\_000

Used to inform the DMC that a particular queue (RAM) entry has failed, where 0 means failed and not included for allocation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue\_allocate\_control\_031\_000 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x148  
**Type** Read-write  
**Reset** 0xFFFFFFFF  
**Width** 32

### 3.3.79 queue\_allocate\_control\_063\_032

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue\_allocate\_control\_063\_032 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x14C  
**Type** Read-write  
**Reset** 0xFFFFFFFF  
**Width** 32

### 3.3.80 queue\_allocate\_control\_095\_064

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue\_allocate\_control\_095\_064 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x150
<b>Type</b>	Read-write
<b>Reset</b>	0xFFFFFFFF
<b>Width</b>	32

### 3.3.81 queue\_allocate\_control\_127\_096

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue\_allocate\_control\_127\_096 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x154
<b>Type</b>	Read-write
<b>Reset</b>	0xFFFFFFFF
<b>Width</b>	32

### 3.3.82 link\_err\_count

Counter register for link errors. The counter increments on detection of a new link error (dfi\_alert\_n or dfi\_err). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The link\_err\_count register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x16C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.83 scrub\_control0\_next

Scrub engine channel control register. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub\_control0\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x170
<b>Type</b>	Read-write
<b>Reset</b>	0x0FFFFFF0
<b>Width</b>	32

### 3.3.84 scrub\_address\_min0\_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub\_address\_min0\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x174
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.85 scrub\_address\_max0\_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub\_address\_max0\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x178
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.86 scrub\_address\_current0

Current scrub address for scrub 0. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The scrub\_address\_current0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x17C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.87 scrub\_control1\_next

Scrub engine channel control register. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub\_control1\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x180
<b>Type</b>	Read-write
<b>Reset</b>	0x0FFFFFF0
<b>Width</b>	32

### 3.3.88 scrub\_address\_min1\_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub\_address\_min1\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x184
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.89 scrub\_address\_max1\_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub\_address\_max1\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x188
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.90 scrub\_address\_current1

Current scrub address for scrub 1. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The scrub\_address\_current1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x18C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.91 cs\_remap\_control\_31\_00\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs\_remap\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1A0
<b>Type</b>	Read-write
<b>Reset</b>	0x00020001
<b>Width</b>	32

### 3.3.92 cs\_remap\_control\_63\_32\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs\_remap\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1A4
<b>Type</b>	Read-write
<b>Reset</b>	0x00080004
<b>Width</b>	32

### 3.3.93 cs\_remap\_control\_95\_64\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs\_remap\_control\_95\_64\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1A8
<b>Type</b>	Read-write
<b>Reset</b>	0x00200010
<b>Width</b>	32

### 3.3.94 cs\_remap\_control\_127\_96\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs\_remap\_control\_127\_96\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1AC
<b>Type</b>	Read-write
<b>Reset</b>	0x00800040
<b>Width</b>	32

### 3.3.95 cid\_remap\_control\_31\_00\_next

Control register for dfi\_CID remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cid\_remap\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1B0
<b>Type</b>	Read-write
<b>Reset</b>	0x20001000
<b>Width</b>	32

### 3.3.96 cid\_remap\_control\_63\_32\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cid\_remap\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1B4
<b>Type</b>	Read-write
<b>Reset</b>	0x00004000
<b>Width</b>	32

### 3.3.97 cke\_remap\_control\_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cke\_remap\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1C0
<b>Type</b>	Read-write
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.98 rst\_remap\_control\_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rst\_remap\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1C4
<b>Type</b>	Read-write
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.99 ck\_remap\_control\_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The ck\_remap\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes



<b>Offset</b>	0x1C8
<b>Type</b>	Read-write
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.100 power\_group\_control\_31\_00\_next

Power Group Control register for power managing ranks together. The ranks that are CKE-tied together as represented in cke\_remap\_control register should belong to the same power-group Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power\_group\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1D0
<b>Type</b>	Read-write
<b>Reset</b>	0x00020001
<b>Width</b>	32

### 3.3.101 power\_group\_control\_63\_32\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power\_group\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1D4
<b>Type</b>	Read-write
<b>Reset</b>	0x00080004
<b>Width</b>	32

### 3.3.102 power\_group\_control\_95\_64\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power\_group\_control\_95\_64\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1D8
<b>Type</b>	Read-write
<b>Reset</b>	0x00200010
<b>Width</b>	32

### 3.3.103 power\_group\_control\_127\_96\_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power\_group\_control\_127\_96\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1DC
<b>Type</b>	Read-write
<b>Reset</b>	0x00800040
<b>Width</b>	32

### 3.3.104 phy\_rdwrdata\_cs\_mask\_31\_00

Maps a logical rank to the physical rank phy\_rd/wrdata\_cs output pins. Using this register it is possible to map a logical rank to multiple phy\_rdwrdata\_cs output pins. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy\_rdwrdata\_cs\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1E0
<b>Type</b>	Read-write
<b>Reset</b>	0xF7BFDFFE
<b>Width</b>	32

### 3.3.105 phy\_rdwrdata\_cs\_mask\_63\_32

Maps a logical rank to the physical rank phy\_rd/wrdata\_cs output pins. Using this register it is possible to map a logical rank to multiple phy\_rdwrdata\_cs output pins. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy\_rdwrdata\_cs\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1E4
<b>Type</b>	Read-write
<b>Reset</b>	0x7BFDFFEF
<b>Width</b>	32

### 3.3.106 phy\_request\_cs\_remap

Maps PHY training request from a physical chip select to DMC internal logical chip select. Requests which are mapped using this register are dfi\_rdlvl\_cs, dfi\_rdlvl\_gate\_cs, dfi\_wrlvl\_cs, dfi\_phylvl\_req\_cs\_n and dfi\_phymstr\_cs\_state. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy\_request\_cs\_remap register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1E8
<b>Type</b>	Read-write
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.107 feature\_control\_next

Control register for DMC features. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The feature\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1F0
<b>Type</b>	Read-write
<b>Reset</b>	0x0AA00000
<b>Width</b>	32

### 3.3.108 mux\_control\_next

Control muxing options for the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The mux\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1F4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.109 rank\_remap\_control\_next

Control register for rank remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rank\_remap\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1F8
<b>Type</b>	Read-write
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.110 t\_refi\_next

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_refi\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x200
<b>Type</b>	Read-write
<b>Reset</b>	0x00090100
<b>Width</b>	32

### 3.3.111 t\_rfc\_next

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rfc\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x204
<b>Type</b>	Read-write
<b>Reset</b>	0x00008C23
<b>Width</b>	32

### 3.3.112 t\_mrr\_next

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note:

this value is used to determine the data cycles returned as a result of an MRR command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_mrr\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x208
<b>Type</b>	Read-write
<b>Reset</b>	0x00000002
<b>Width</b>	32

### 3.3.113 t\_mrw\_next

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_mrw\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x20C
<b>Type</b>	Read-write
<b>Reset</b>	0x0000000C
<b>Width</b>	32

### 3.3.114 t\_rcd\_next

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rcd\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x218
<b>Type</b>	Read-write
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.115 t\_ras\_next

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_ras\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x21C
<b>Type</b>	Read-write
<b>Reset</b>	0x0000000E
<b>Width</b>	32

### 3.3.116 t\_rp\_next

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rp\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x220
<b>Type</b>	Read-write
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.117 t\_rpall\_next

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rpall\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x224
<b>Type</b>	Read-write
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.118 t\_rrd\_next

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The `_l` and `_s` fields apply to the same bank group, a different bank group, and different logical rank, respectively, as described in the DDR4 specification. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_rrd_next` register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x228
<b>Type</b>	Read-write
<b>Reset</b>	0x04000404
<b>Width</b>	32

### 3.3.119 t\_act\_window\_next

Configures the tFAW and tMAWi timing parameters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_act_window_next` register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x22C
<b>Type</b>	Read-write
<b>Reset</b>	0x03561414
<b>Width</b>	32

### 3.3.120 t\_rtr\_next

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (`t_rtr_s`), same chip, same bank group (`t_rtr_l`), different chip-selects (`t_rtr_cs`), and same chip, different logical rank (`t_rtr_dlr`). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_rtr_next` register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x234
<b>Type</b>	Read-write
<b>Reset</b>	0x10060404
<b>Width</b>	32

**3.3.121 t\_rtw\_next**

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t\_rtw\_s), same chip, same bank group (t\_trw\_l), and other chip-selects (t\_rtw\_cs). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rtw\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x238
<b>Type</b>	Read-write
<b>Reset</b>	0x00060606
<b>Width</b>	32

**3.3.122 t\_rtp\_next**

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rtp\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x23C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000004
<b>Width</b>	32

**3.3.123 t\_wr\_next**

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITES, to the same bank. Note: this must take into account CRC timing requirements. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_wr\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x244
<b>Type</b>	Read-write
<b>Reset</b>	0x00000005
<b>Width</b>	32



**3.3.124 t\_wtr\_next**

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR\_s), same chip, same bank group (t\_WTR\_l), and alternate chip (tWTR\_cs). Note: these must take into account CRC timing requirements. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_wtr\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x248
<b>Type</b>	Read-write
<b>Reset</b>	0x00040505
<b>Width</b>	32

**3.3.125 t\_wtw\_next**

Configures the write-to-write timing parameter for same chip, other bank group (t\_wtw\_s), same chip, same bank group (t\_wtw\_l), alternate chip (t\_wtw\_cs) writes, same chip, different logical rank(t\_wtw\_dlr). Note: these must take into account CRC timing requirements. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_wtw\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x24C
<b>Type</b>	Read-write
<b>Reset</b>	0x10060404
<b>Width</b>	32

**3.3.126 t\_xmpd\_next**

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_xmpd\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x254
<b>Type</b>	Read-write
<b>Reset</b>	0x000003FF
<b>Width</b>	32

### 3.3.127 t\_ep\_next

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge powerdownrequest and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_ep\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x258
<b>Type</b>	Read-write
<b>Reset</b>	0x00000002
<b>Width</b>	32

### 3.3.128 t\_xp\_next

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t\_xpdll must be greater than or equal to tRCD and tCKE, and t\_xp must be greater than or equal to tMPX\_S. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_xp\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x25C
<b>Type</b>	Read-write
<b>Reset</b>	0x00060002
<b>Width</b>	32

### 3.3.129 t\_esr\_next

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_esr\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x260
<b>Type</b>	Read-write
<b>Reset</b>	0x0000000E
<b>Width</b>	32

**3.3.130 t\_xsr\_next**

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_xsr\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x264
<b>Type</b>	Read-write
<b>Reset</b>	0x05120100
<b>Width</b>	32

**3.3.131 t\_esrck\_next**

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_esrck\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x268
<b>Type</b>	Read-write
<b>Reset</b>	0x00000005
<b>Width</b>	32

**3.3.132 t\_ckxsr\_next**

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_ckxsr\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x26C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.133 t\_cmd\_next

Configures command signaling timing. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_cmd\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x270
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.134 t\_parity\_next

Parity latencies t\_parinlat and t\_completion. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_parity\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x274
<b>Type</b>	Read-write
<b>Reset</b>	0x00000900
<b>Width</b>	32

### 3.3.135 t\_zqcs\_next

Configures the delay to apply following a ZQC-Short calibration command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_zqcs\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x278
<b>Type</b>	Read-write
<b>Reset</b>	0x00000040
<b>Width</b>	32

### 3.3.136 t\_rw\_odt\_clr\_next

This timing parameter applies extra guard-band between the last issued rd/wr command and potential ZQC, SREF, and MRS commands which are issued automatically by hardware such as tpoll. This may be necessary to prevent overlap of these automated commands with ranks actively participating in non-target rank ODT (while other ranks are streaming data). ZQC, MRS, and SREF commands are typically

not allowed on non-target ranks in this case as these commands could change ODT settings. In general, if non-target rank termination is used this parameter should be programmed to `t_odt_off_rd/wr`(max setting) + DODTLoff(from DDR4 spec) Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_rw_odt_clr_next` register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x27C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.137 `t_rddata_en_next`

Determines the time between a READ command commencing on the DFI interface, and the assertion of the `dfi_read_en` signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_rddata_en_next` register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x300
<b>Type</b>	Read-write
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.138 `t_phyrdlat_next`

Determines the maximum possible time between the assertion of the `dfi_read_en` signal, and the assertion of the `dfi_rddata_valid` signal by the PHY. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_phyrdlat_next` register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x304
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.139 t\_phywrlat\_next

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi\_wrddata\_en, dfi\_wrddata\_cs and dfi\_wrddata signals. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_phywrlat\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x308
<b>Type</b>	Read-write
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.140 rdlvl\_control\_next

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rdlvl\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x310
<b>Type</b>	Read-write
<b>Reset</b>	0x00001080
<b>Width</b>	32

### 3.3.141 rdlvl\_mrs\_next

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl\_control register. See the PHY interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rdlvl\_mrs\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x314
<b>Type</b>	Read-write
<b>Reset</b>	0x00000004
<b>Width</b>	32

**3.3.142 t\_rdlvl\_en\_next**

Configures the t\_rdlvl\_en timing parameter. This specifies the cycle delay between asserting dfi\_rdlvl\_en and the first training command, and also the cycle delay between deasserting dfi\_rdlvl\_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rdlvl\_en\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x318
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.143 t\_rdlvl\_rr\_next**

Configures the t\_rdlvl\_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi\_rdlvl\_en after observing dfi\_rdlvl\_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_rdlvl\_rr\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x31C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.144 wrlvl\_control\_next**

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wrlvl\_control\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x320
<b>Type</b>	Read-write
<b>Reset</b>	0x00101000
<b>Width</b>	32

### 3.3.145 wrlvl\_mrs\_next

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl\_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wrlvl\_mrs\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x324
<b>Type</b>	Read-write
<b>Reset</b>	0x00000086
<b>Width</b>	32

### 3.3.146 t\_wrlvl\_en\_next

Configures the t\_wrlvl\_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi\_wrlvl\_en, the delay between asserting dfi\_wrlvl\_en and the first training command, the delay between deasserting dfi\_wrlvl\_en and deassertingODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_wrlvl\_en\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x328
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.147 t\_wrlvl\_ww\_next

Configures the t\_wrlvl\_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and deassertingdfi\_wrlvl\_en on observing dfi\_wrlvl\_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_wrlvl\_ww\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x32C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32



### 3.3.148 training\_wrlvl\_slice\_status

Shows slice information relating to the wrlvl training request status of the DMC. Access restrictions: RO  
Can be read from when in ALL states. Cannot be changed.

The training\_wrlvl\_slice\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x334
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.149 training\_rdlvl\_slice\_status

Shows slice information relating to the rdlvl training request status of the DMC. Access restrictions: RO  
Can be read from when in ALL states. Cannot be changed.

The training\_rdlvl\_slice\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x338
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.150 training\_rdlvl\_gate\_slice\_status

Shows slice information relating to the rdlvl gate training request status of the DMC. Access restrictions: RO  
Can be read from when in ALL states. Cannot be changed.

The training\_rdlvl\_gate\_slice\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x33C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.151 training\_wdqlvl\_slice\_status

Shows slice information relating to the WrDQ training request status of the DMC. Access restrictions: RO  
Can be read from when in ALL states. Cannot be changed.

The training\_wdqlvl\_slice\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x340
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.152 training\_wdqlvl\_slice\_result

Shows per slice result from the PHY in response to the WrDQ training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training\_wdqlvl\_slice\_result register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x344
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.153 phy\_power\_control\_next

Configures the low-power requests made to the PHY for the different channel states. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy\_power\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x348
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.154 t\_lpresp\_next

Configures the minimum cycle delay to apply for PHY low-power handshakes. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_lpresp\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x34C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.155 phy\_update\_control\_next

Configures the update mechanism to use in response to PHY training requests. Access restrictions: RW  
Can be read from when in ALL states. Can be written to when in ALL states.

The phy\_update\_control\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x350
<b>Type</b>	Read-write
<b>Reset</b>	0x2FE00000
<b>Width</b>	32

### 3.3.156 t\_odth\_next

Configures the ODT8 timing parameter as timed from Write command registered with ODT high  
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_odth\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x354
<b>Type</b>	Read-write
<b>Reset</b>	0x00000006
<b>Width</b>	32

### 3.3.157 odt\_timing\_next

Configures the ODT on and off timing. Access restrictions: RW Can be read from when in ALL states.  
Can be written to when in ALL states.

The odt\_timing\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x358
<b>Type</b>	Read-write
<b>Reset</b>	0x06000600
<b>Width</b>	32

### 3.3.158 odt\_wr\_control\_31\_00\_next

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt\_wr\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x360
<b>Type</b>	Read-write
<b>Reset</b>	0x08040201
<b>Width</b>	32

### 3.3.159 odt\_wr\_control\_63\_32\_next

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt\_wr\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x364
<b>Type</b>	Read-write
<b>Reset</b>	0x80402010
<b>Width</b>	32

### 3.3.160 odt\_rd\_control\_31\_00\_next

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt\_rd\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x368
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.161 odt\_rd\_control\_63\_32\_next

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt\_rd\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x36C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.162 temperature\_readout

Holds the status of the temperature information. Reading the register returns the current temperature from the most recent automated temperature poll. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The temperature\_readout register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x370
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.163 training\_status

Shows information relating to the training request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x378
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.164 training\_status\_63\_32

Shows information relating to the update request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training\_status\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x37C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.165 dq\_map\_control\_15\_00\_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq\_map\_control\_15\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x380
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.166 dq\_map\_control\_31\_16\_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq\_map\_control\_31\_16\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x384
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.167 dq\_map\_control\_47\_32\_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq\_map\_control\_47\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x388
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.168 dq\_map\_control\_63\_48\_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq\_map\_control\_63\_48\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x38C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.169 dq\_map\_control\_71\_64\_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq\_map\_control\_71\_64\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x390
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.170 rank\_status

Shows the current status of geardown, MPD and CAL. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The rank\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x398
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.171 mode\_change\_status

Shows the current status of the sequence that is currently being processed. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The mode\_change\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x39C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.172 odt\_cp\_control\_31\_00\_next

Determines which of the 8 dfi\_odt[7:0] output signals are connected to a logically addressed rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt\_cp\_control\_31\_00\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x3B0
<b>Type</b>	Read-write
<b>Reset</b>	0x08040201
<b>Width</b>	32

### 3.3.173 odt\_cp\_control\_63\_32\_next

Determines which of the 8 dfi\_odt[7:0] output signals are driven during a write to DRAM. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt\_cp\_control\_63\_32\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x3B4
<b>Type</b>	Read-write



**Reset** 0x80402010  
**Width** 32

### 3.3.174 user\_status

Shows the value of the input user\_status signals. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The user\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x400  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.175 user\_config0\_next

Drives the output user\_config0 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user\_config0\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x408  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.176 user\_config1\_next

Drives the output user\_config1 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user\_config1\_next register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x40C  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.177 user\_config2

Drives the output user\_config2 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user\_config2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x410
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.178 user\_config3

Drives the output user\_config3 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user\_config3 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x414
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.179 interrupt\_control

Configures interrupt behavior. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The interrupt\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x500
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.180 interrupt\_clr

Clear register for interrupts. Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The interrupt\_clr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x508
<b>Type</b>	Write-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.181 interrupt\_status

Status register for interrupts (pre-mask). Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The interrupt\_status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x510
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.182 failed\_access\_int\_info\_31\_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed\_access\_int\_info\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x538
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.183 failed\_access\_int\_info\_63\_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed\_access\_int\_info\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x53C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.184 failed\_prog\_int\_info\_31\_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed\_prog\_int\_info\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x540
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.185 failed\_prog\_int\_info\_63\_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed\_prog\_int\_info\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x544
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.186 link\_err\_int\_info\_31\_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The link\_err\_int\_info\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x548
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.187 link\_err\_int\_info\_63\_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The link\_err\_int\_info\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x54C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.188 arch\_fsm\_int\_info\_31\_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The arch\_fsm\_int\_info\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x550
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.189 arch\_fsm\_int\_info\_63\_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The arch\_fsm\_int\_info\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x554
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.190 t\_db\_train\_resp\_next

Configures the t\_db\_train\_resp timing parameter for DB-DRAM Training. With DFI4.0 PHY this register is specified to define the cycle delay between DFI read command and when the response is valid on the dfi\_db\_train\_resp. However this register can also be configured in DFI3.1 mode (optional: in absence of dfi\_rddata\_valid) to define the delay between DFI read command and when the response is

valid on the dfi\_rddata. This must include the whole round trip time including the board delays, take a look at DFI4.0 spec for details. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_db\_train\_resp\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x610
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.191 t\_lvl\_disconnect\_next

Configures the t\_lvl\_disconnect timing parameter for all DFI training interfaces. This value should be programmed to be max of all t\*lvl\_disconnect and t\*lvl\_disconnect\_error timing parameters from the PHY Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t\_lvl\_disconnect\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x614
<b>Type</b>	Read-write
<b>Reset</b>	0x0000000F
<b>Width</b>	32

### 3.3.192 wdqlvl\_control\_next

Determines the DMC behavior during write-DQ training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl\_control\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x620
<b>Type</b>	Read-write
<b>Reset</b>	0x00000094
<b>Width</b>	32

### 3.3.193 wdqlvl\_vrefdq\_train\_mrs\_next

Determines the Mode Register command to use to place the DRAM into a VrefDQ training mode as part of WrDQ training, when enabled by the wdqlvl\_control register. You enable this function with the

wdqlvl\_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl\_vrefdq\_train\_mrs\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x624
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.194 wdqlvl\_address\_31\_00\_next

Programs the row and column address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl\_address\_31\_00\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x628
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.195 wdqlvl\_address\_63\_32\_next

Programs the address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl\_address\_63\_32\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x62C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.196 t\_wdqlvl\_en\_next

Configures the t\_wdqlvl\_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi\_wdqlvl\_en, the delay between asserting dfi\_wdqlvl\_en and the first training command, the delay between deasserting dfi\_wdqlvl\_en and deassertingODT, and deassertingODT to any

subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_wdqlvl_en_next` register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x630
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.197 `t_wdqlvl_ww_next`

Configures the `t_wdqlvl_ww` timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and deasserting `dfi_wrlvl_en` on observing `dfi_wdqlvl_resp`. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_wdqlvl_ww_next` register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x634
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.198 `t_wdqlvl_rw_next`

Configures the `t_wdqlvl_rw` timing parameter. Specifies the minimum numbers of clock cycles from the last read in a calibration sequence to the first write in the next set of calibration commands. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `t_wdqlvl_rw_next` register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x638
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.199 `training_wdqlvl_slice_resp`

Shows per slice response from the PHY in response to the WrDQ training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.



The training\_wdqlvl\_slice\_resp register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x63C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.200 training\_rdlvl\_slice\_resp

Shows per slice response from the PHY in response to the rdlvl training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training\_rdlvl\_slice\_resp register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x640
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.201 phymstr\_control\_next

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phymstr\_control\_next register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x654
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.202 err0fr

This record defines features which are common to all RAS error records in this section. Each field defines which of the architecturally-defined common features are implemented and, of the implemented features, which are software programmable. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err0fr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x700
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.203 err0ctrl0

This register is the global control register for the DMC RAS functions. This register control features such as ECC type and enable, error reporting and interrupt enable, error deferment, etc. The setting of a Global control record bit affects all records. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The err0ctrl0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x708
<b>Type</b>	Read-write
<b>Reset</b>	0x00000010
<b>Width</b>	32

### 3.3.204 err0ctrl1

This register is the global control register for the DMC RAS functions. The registers in this record affect all DMC RAS records. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The err0ctrl1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x70C
<b>Type</b>	Read-write
<b>Reset</b>	0x000000C0
<b>Width</b>	32

### 3.3.205 err0status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err0status register characteristics are:

#### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x710
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.206 err1fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err1fr register characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x740
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.207 err1ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err1ctlr register characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x748
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.208 err1status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1status register characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x750
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.209 err1addr0

Contains the physical address LSB's associated with the error. If an error has an associated physical address, this must be written to the address register when the error is recorded. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1addr0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x758
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.210 err1addr1

Contains the physical address MSB's associated with the error. If an error has an associated physical address, this must be written to the address register when the error is recorded. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1addr1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x75C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.211 err1misc0

This register gives the Physical Rank, Row, and Column of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x760
<b>Type</b>	Read-write

**Reset** 0x00000000  
**Width** 32

### 3.3.212 err1misc1

This register gives the bank, logical rank, and failed nibble location of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x764  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.213 err1misc2

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x768  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.214 err1misc3

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc3 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x76C  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.215 err1misc4

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc4 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x770
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.216 err1misc5

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc5 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x774
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.217 err2fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err2fr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x780
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.218 err2ctrlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTRLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err2ctrl register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x788
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.219 err2status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2status register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x790
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.220 err2addr0

Contains the physical address LSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2addr0 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x798
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.221 err2addr1

Contains the physical address MSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2addr1 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x79C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.222 err2misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7A0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.223 err2misc1

This register gives the bank and logical rank of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7A4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.224 err2misc2

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7A8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000



**Width** 32

### 3.3.225 err2misc3

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.  
Can be written to when in ALL states.

The err2misc3 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7AC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.226 err2misc4

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.  
Can be written to when in ALL states.

The err2misc4 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7B0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.227 err2misc5

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states.  
Can be written to when in ALL states.

The err2misc5 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7B4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.228 err3fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3fr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7C0
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.229 err3ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3ctlr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7C8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.230 err3status

This status register reports error type, status, and contains valid bits for extra syndrome registers Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x7D0
<b>Type</b>	Read-write
<b>Reset</b>	0x000000
<b>Width</b>	32

### 3.3.231 err3addr0

Contains the physical address LSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3addr0 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x7D8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.232 err3addr1

Contains the physical address MSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3addr1 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x7DC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.233 err4fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err4fr register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x800
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.234 err4ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err4ctlr register characteristics are:

**Usage constraints**

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x808
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.235 err4status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4status register characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x810
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.236 err4addr0

Contains the physical address LSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4addr0 register characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x818
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.237 err4addr1

Contains the physical address MSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4addr1 register characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

There is only one DMC configuration.

### Attributes

<b>Offset</b>	0x81C
<b>Type</b>	Read-write

**Reset** 0x00000000  
**Width** 32

### 3.3.238 err4misc0

This register gives the Physical Rank, Row, and Column of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x820  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.239 err4misc1

This register gives the bank and logical rank, and DBID of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x824  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.240 err4misc2

Ram Correctable Error Counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x828  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.241 err5fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err5fr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x840
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.242 err5ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err5ctlr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x848
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.243 err5status

This status register reports error type, status, and contains valid bits for extra syndrome registers Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x850
<b>Type</b>	Read-write
<b>Reset</b>	0x000000
<b>Width</b>	32

### 3.3.244 err5addr0

Contains the physical address LSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5addr0 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x858
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.245 err5addr1

Contains the physical address MSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5addr1 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x85C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.246 err5misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc0 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x860
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.247 err5misc1

This register gives the bank and logical rank, and DBID of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc1 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x864
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.248 err5misc2

RAM Uncorrectable error counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x868
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.249 err6fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err6fr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x880
<b>Type</b>	Read-only
<b>Reset</b>	0x000009AA
<b>Width</b>	32

### 3.3.250 err6ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err6ctlr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x888
<b>Type</b>	Read-only



**Reset** 0x00000000  
**Width** 32

### 3.3.251 err6status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6status register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x890  
**Type** Read-write  
**Reset** 0x000000  
**Width** 32

### 3.3.252 err6addr0

Contains the physical address LSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6addr0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x898  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.253 err6addr1

Contains the physical address MSB's associated with the error. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6addr1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x89C  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.254 err6misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared.  
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6misc0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x8A0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.255 err6misc1

This register gives the bank and logical rank, and DBID of the first error detected since the last clear.  
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6misc1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x8A4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.256 errgsr

This register shows the status of all the DMC error records. When a CFH, FH, or ER interrupt occurs software may check this register to tell which error record(s) caused the interrupt. Each field in this register is a copy of each individual records ERRnSTATUS.V bit. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The errgsr register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x920
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.257 pmu\_snapshot\_req

Generates PMU snapshot request Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The pmu\_snapshot\_req register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA00
<b>Type</b>	Write-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.258 pmu\_snapshot\_ack

Indicates PMU snapshot acknowledge Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_snapshot\_ack register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA04
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.259 pmu\_overflow\_status\_clkdiv2

Indicates which clkdiv2 counters have overflowed Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_overflow\_status\_clkdiv2 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA08
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.260 pmu\_overflow\_status\_clk

Indicates which clk domain counters have overflowed Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_overflow\_status\_clk register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA0C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.261 pmu\_clkdiv2\_counter\_0\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_0\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA10
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.262 pmu\_clkdiv2\_counter\_0\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_0\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA14
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.263 pmu\_clkdiv2\_counter\_0\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_0\_match\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA18
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000

**Width** 32

### 3.3.264 pmu\_clkdiv2\_counter\_0\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_0\_match\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0xA1C  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.265 pmu\_clkdiv2\_counter\_0\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_0\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0xA20  
**Type** Read-write  
**Reset** 0x00000000  
**Width** 32

### 3.3.266 pmu\_clkdiv2\_counter\_0\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_0\_snapshot\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0xA28  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.267 pmu\_clkdiv2\_counter\_0\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_0\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA30
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.268 pmu\_clkdiv2\_counter\_1\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_1\_mask\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA38
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.269 pmu\_clkdiv2\_counter\_1\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_1\_mask\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA3C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.270 pmu\_clkdiv2\_counter\_1\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_1\_match\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA40
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.271 pmu\_clkdiv2\_counter\_1\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_1\_match\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA44
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.272 pmu\_clkdiv2\_counter\_1\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_1\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA48
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.273 pmu\_clkdiv2\_counter\_1\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_1\_snapshot\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA50
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000

**Width** 32

### 3.3.274 pmu\_clkdiv2\_counter\_1\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_1\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA58
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.275 pmu\_clkdiv2\_counter\_2\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_2\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA60
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.276 pmu\_clkdiv2\_counter\_2\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_2\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA64
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.277 pmu\_clkdiv2\_counter\_2\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.



The pmu\_clkdiv2\_counter\_2\_match\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA68
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.278 pmu\_clkdiv2\_counter\_2\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_2\_match\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA6C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.279 pmu\_clkdiv2\_counter\_2\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_2\_control register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xA70
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.280 pmu\_clkdiv2\_counter\_2\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_2\_snapshot\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA78
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.281 pmu\_clkdiv2\_counter\_2\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_2\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA80
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.282 pmu\_clkdiv2\_counter\_3\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_3\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA88
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.283 pmu\_clkdiv2\_counter\_3\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_3\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA8C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000

**Width** 32

### 3.3.284 pmu\_clkdiv2\_counter\_3\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter.  
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_3\_match\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA90
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.285 pmu\_clkdiv2\_counter\_3\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_3\_match\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA94
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.286 pmu\_clkdiv2\_counter\_3\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_3\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xA98
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.287 pmu\_clkdiv2\_counter\_3\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states.  
Cannot be changed.

The pmu\_clkdiv2\_counter\_3\_snapshot\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xAA0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.288 pmu\_clkdiv2\_counter\_3\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_3\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xAA8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.289 pmu\_clkdiv2\_counter\_4\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_4\_mask\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xAB0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.290 pmu\_clkdiv2\_counter\_4\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_4\_mask\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAB4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.291 pmu\_clkdiv2\_counter\_4\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter.  
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_4\_match\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAB8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.292 pmu\_clkdiv2\_counter\_4\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_4\_match\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xABC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.293 pmu\_clkdiv2\_counter\_4\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_4\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAC0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000

**Width** 32

### 3.3.294 pmu\_clkdiv2\_counter\_4\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_4\_snapshot\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAC8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.295 pmu\_clkdiv2\_counter\_4\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_4\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAD0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.296 pmu\_clkdiv2\_counter\_5\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_5\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAD8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.297 pmu\_clkdiv2\_counter\_5\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_5\_mask\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xADC
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.298 pmu\_clkdiv2\_counter\_5\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter.  
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_5\_match\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xAE0
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.299 pmu\_clkdiv2\_counter\_5\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_5\_match\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xAE4
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.300 pmu\_clkdiv2\_counter\_5\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_5\_control register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAE8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.301 pmu\_clkdiv2\_counter\_5\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_5\_snapshot\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAF0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.302 pmu\_clkdiv2\_counter\_5\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_5\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xAF8
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.303 pmu\_clkdiv2\_counter\_6\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_6\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB00
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000



**Width** 32

### 3.3.304 pmu\_clkdiv2\_counter\_6\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_6\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB04
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.305 pmu\_clkdiv2\_counter\_6\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_6\_match\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB08
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.306 pmu\_clkdiv2\_counter\_6\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_6\_match\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB0C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.307 pmu\_clkdiv2\_counter\_6\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_6\_control register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB10
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.308 pmu\_clkdiv2\_counter\_6\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_6\_snapshot\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB18
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.309 pmu\_clkdiv2\_counter\_6\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_6\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB20
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.310 pmu\_clkdiv2\_counter\_7\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_7\_mask\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB28
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.311 pmu\_clkdiv2\_counter\_7\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_7\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB2C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.312 pmu\_clkdiv2\_counter\_7\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_7\_match\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB30
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.313 pmu\_clkdiv2\_counter\_7\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_7\_match\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB34
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000

**Width** 32

### 3.3.314 pmu\_clkdiv2\_counter\_7\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_7\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB38
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.315 pmu\_clkdiv2\_counter\_7\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clkdiv2\_counter\_7\_snapshot\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB40
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.316 pmu\_clkdiv2\_counter\_7\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clkdiv2\_counter\_7\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB48
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.317 pmu\_clk\_counter\_0\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_0\_mask\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB50
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.318 pmu\_clk\_counter\_0\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_0\_mask\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB54
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.319 pmu\_clk\_counter\_0\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_0\_match\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB58
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.320 pmu\_clk\_counter\_0\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_0\_match\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB5C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.321 pmu\_clk\_counter\_0\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_0\_control register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB60
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.322 pmu\_clk\_counter\_0\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clk\_counter\_0\_snapshot\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB68
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.323 pmu\_clk\_counter\_0\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_0\_value\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB70
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000

**Width** 32

### 3.3.324 pmu\_clk\_counter\_1\_mask\_31\_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_1\_mask\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB78
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.325 pmu\_clk\_counter\_1\_mask\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_1\_mask\_63\_32 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB7C
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.326 pmu\_clk\_counter\_1\_match\_31\_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_1\_match\_31\_00 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xB80
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.327 pmu\_clk\_counter\_1\_match\_63\_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_1\_match\_63\_32 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB84
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.328 pmu\_clk\_counter\_1\_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_1\_control register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB88
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.329 pmu\_clk\_counter\_1\_snapshot\_value\_31\_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu\_clk\_counter\_1\_snapshot\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0xB90
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.330 pmu\_clk\_counter\_1\_value\_31\_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu\_clk\_counter\_1\_value\_31\_00 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.



#### Attributes

<b>Offset</b>	0xB98
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.331 integ\_cfg

Integration test register to enable integration test mode. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The integ\_cfg register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xE00
<b>Type</b>	Read-write
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.332 integ\_outputs

Drives the value of outputs when in integration test mode. Access restrictions: WO Cannot be read from. Can be written to when in CONFIG or LOW-POWER states.

The integ\_outputs register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0xE08
<b>Type</b>	Write-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.333 address\_control\_now

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The address\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1010
<b>Type</b>	Read-only
<b>Reset</b>	0x00030202

**Width** 32

### 3.3.334 decode\_control\_now

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, cid, bank, row, and the column address. Note: Order fields must be unique, ie. row\_order != bank\_order != rank\_order. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The decode\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x1014  
**Type** Read-only  
**Reset** 0x001A3000  
**Width** 32

### 3.3.335 address\_map\_now

Configures the system address mapping options. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The address\_map\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x101C  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.336 low\_power\_control\_now

Configures the low-power features of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The low\_power\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x1020  
**Type** Read-only  
**Reset** 0x00000020  
**Width** 32

### 3.3.337 turnaround\_control\_now

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The turnaround\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1028
<b>Type</b>	Read-only
<b>Reset</b>	0x0F0F0F0F
<b>Width</b>	32

### 3.3.338 hit\_turnaround\_control\_now

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The hit\_turnaround\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x102C
<b>Type</b>	Read-only
<b>Reset</b>	0x08909FBF
<b>Width</b>	32

### 3.3.339 qos\_class\_control\_now

Configures the priority class for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qos\_class\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1030
<b>Type</b>	Read-only
<b>Reset</b>	0x00000FC8
<b>Width</b>	32

### 3.3.340 escalation\_control\_now

Configures the settings for escalating the priority of entries in the queue. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The escalation\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1034
<b>Type</b>	Read-only
<b>Reset</b>	0x00080F03
<b>Width</b>	32

### 3.3.341 qv\_control\_31\_00\_now

Configures the priority settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qv\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1038
<b>Type</b>	Read-only
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.342 qv\_control\_63\_32\_now

Configures the priority settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qv\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x103C
<b>Type</b>	Read-only
<b>Reset</b>	0xFEDCBA98
<b>Width</b>	32

### 3.3.343 rt\_control\_31\_00\_now

Configures the timeout settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rt\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1040
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.344 rt\_control\_63\_32\_now

Configures the timeout settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rt\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1044
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.345 timeout\_control\_now

Configures the prescaler applied to timeout values. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The timeout\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1048
<b>Type</b>	Read-only
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.346 credit\_control\_now

Configures the settings for preventing starvation of CHI protocol retries. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The credit\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x104C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000F03
<b>Width</b>	32

### 3.3.347 write\_priority\_control\_31\_00\_now

Configures the priority settings for write requests within the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The write\_priority\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1050
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.348 write\_priority\_control\_63\_32\_now

Configures the priority settings for write requests within the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The write\_priority\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1054
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.349 queue\_threshold\_control\_31\_00\_now

Configures the threshold settings for requests in the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The queue\_threshold\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1058
<b>Type</b>	Read-only
<b>Reset</b>	0x00000008
<b>Width</b>	32

### 3.3.350 queue\_threshold\_control\_63\_32\_now

Configures the threshold settings for requests in the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The queue\_threshold\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x105C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.351 address\_shutter\_31\_00\_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address\_shutter\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1060
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.352 address\_shutter\_63\_32\_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address\_shutter\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1064
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.353 address\_shutter\_95\_64\_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address\_shutter\_95\_64\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1068
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.354 address\_shutter\_127\_96\_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address\_shutter\_127\_96\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x106C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32



### 3.3.355 address\_shutter\_159\_128\_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address\_shutter\_159\_128\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1070
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.356 address\_shutter\_191\_160\_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address\_shutter\_191\_160\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1074
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.357 memory\_address\_max\_31\_00\_now

Configures the address space control for the DMC default region. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The memory\_address\_max\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1078
<b>Type</b>	Read-only
<b>Reset</b>	0x00000010
<b>Width</b>	32

### 3.3.358 memory\_address\_max\_47\_32\_now

Configures the address space control for the DMC default region. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The memory\_address\_max\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x107C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.359 access\_address\_min0\_31\_00\_now

Configures the address space control for address region 0. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min0\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1080
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.360 access\_address\_min0\_47\_32\_now

Configures the address space control for address region 0. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min0\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1084
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.361 access\_address\_max0\_31\_00\_now

Configures the address space control for address region 0. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max0\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1088
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.362 access\_address\_max0\_47\_32\_now

Configures the address space control for address region 0. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max0\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x108C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.363 access\_address\_min1\_31\_00\_now

Configures the address space control for address region 1. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min1\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1090
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.364 access\_address\_min1\_47\_32\_now

Configures the address space control for address region 1. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min1\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1094
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.365 access\_address\_max1\_31\_00\_now

Configures the address space control for address region 1. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max1\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1098
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.366 access\_address\_max1\_47\_32\_now

Configures the address space control for address region 1. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max1\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x109C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.367 access\_address\_min2\_31\_00\_now

Configures the address space control for address region 2. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min2\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10A0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.368 access\_address\_min2\_47\_32\_now

Configures the address space control for address region 2. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min2\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10A4
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.369 access\_address\_max2\_31\_00\_now

Configures the address space control for address region 2. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max2\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10A8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.370 access\_address\_max2\_47\_32\_now

Configures the address space control for address region 2. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max2\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10AC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.371 access\_address\_min3\_31\_00\_now

Configures the address space control for address region 3. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min3\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10B0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.372 access\_address\_min3\_47\_32\_now

Configures the address space control for address region 3. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min3\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10B4
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.373 access\_address\_max3\_31\_00\_now

Configures the address space control for address region 3. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max3\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10B8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.374 access\_address\_max3\_47\_32\_now

Configures the address space control for address region 3. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max3\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10BC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.375 access\_address\_min4\_31\_00\_now

Configures the address space control for address region 4. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min4\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10C0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.376 access\_address\_min4\_47\_32\_now

Configures the address space control for address region 4. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min4\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10C4
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.377 access\_address\_max4\_31\_00\_now

Configures the address space control for address region 4. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max4\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10C8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.378 access\_address\_max4\_47\_32\_now

Configures the address space control for address region 4. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max4\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10CC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32



### 3.3.379 access\_address\_min5\_31\_00\_now

Configures the address space control for address region 5. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min5\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10D0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.380 access\_address\_min5\_47\_32\_now

Configures the address space control for address region 5. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min5\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10D4
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.381 access\_address\_max5\_31\_00\_now

Configures the address space control for address region 5. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max5\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10D8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.382 access\_address\_max5\_47\_32\_now

Configures the address space control for address region 5. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max5\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10DC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.383 access\_address\_min6\_31\_00\_now

Configures the address space control for address region 6. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min6\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10E0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.384 access\_address\_min6\_47\_32\_now

Configures the address space control for address region 6. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min6\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10E4
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.385 access\_address\_max6\_31\_00\_now

Configures the address space control for address region 6. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max6\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10E8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.386 access\_address\_max6\_47\_32\_now

Configures the address space control for address region 6. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max6\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10EC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.387 access\_address\_min7\_31\_00\_now

Configures the address space control for address region 7. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min7\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10F0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.388 access\_address\_min7\_47\_32\_now

Configures the address space control for address region 7. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_min7\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10F4
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.389 access\_address\_max7\_31\_00\_now

Configures the address space control for address region 7. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max7\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10F8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.390 access\_address\_max7\_47\_32\_now

Configures the address space control for the address region 7. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access\_address\_max7\_47\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x10FC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.391 dci\_replay\_type\_now

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The dci\_replay\_type\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1110
<b>Type</b>	Read-only
<b>Reset</b>	0x00000002
<b>Width</b>	32

### 3.3.392 direct\_control\_now

Represents the training configuration of the DMC executed by a direct command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The direct\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1114
<b>Type</b>	Read-only
<b>Reset</b>	0x0003FFFF
<b>Width</b>	32

### 3.3.393 refresh\_control\_now

Configures the type of refresh commands issued by the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or PAUSED states.

The refresh\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1120
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.394 memory\_type\_now

Configures the DMC for the attached memory type. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The memory\_type\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1128
<b>Type</b>	Read-only
<b>Reset</b>	0x00000101
<b>Width</b>	32

### 3.3.395 scrub\_control0\_now

Scrub engine channel control register. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The scrub\_control0\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1170
<b>Type</b>	Read-only
<b>Reset</b>	0x0FFFFFF0
<b>Width</b>	32

### 3.3.396 scrub\_address\_min0\_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub\_address\_min0\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1174
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.397 scrub\_address\_max0\_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub\_address\_max0\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1178
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.398 scrub\_control1\_now

Scrub engine channel control register. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The scrub\_control1\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1180
<b>Type</b>	Read-only
<b>Reset</b>	0x0FFFFFF0
<b>Width</b>	32

### 3.3.399 scrub\_address\_min1\_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub\_address\_min1\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1184
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.400 scrub\_address\_max1\_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub\_address\_max1\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1188
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.401 cs\_remap\_control\_31\_00\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs\_remap\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11A0
<b>Type</b>	Read-only
<b>Reset</b>	0x00020001
<b>Width</b>	32

### 3.3.402 cs\_remap\_control\_63\_32\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs\_remap\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11A4
<b>Type</b>	Read-only
<b>Reset</b>	0x00080004
<b>Width</b>	32

### 3.3.403 cs\_remap\_control\_95\_64\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs\_remap\_control\_95\_64\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11A8
<b>Type</b>	Read-only
<b>Reset</b>	0x00200010
<b>Width</b>	32



#### 3.3.404 cs\_remap\_control\_127\_96\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs\_remap\_control\_127\_96\_now register characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

There is only one DMC configuration.

##### Attributes

<b>Offset</b>	0x11AC
<b>Type</b>	Read-only
<b>Reset</b>	0x00800040
<b>Width</b>	32

#### 3.3.405 cid\_remap\_control\_31\_00\_now

Control register for dfi\_CID remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cid\_remap\_control\_31\_00\_now register characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

There is only one DMC configuration.

##### Attributes

<b>Offset</b>	0x11B0
<b>Type</b>	Read-only
<b>Reset</b>	0x20001000
<b>Width</b>	32

#### 3.3.406 cid\_remap\_control\_63\_32\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cid\_remap\_control\_63\_32\_now register characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

There is only one DMC configuration.

##### Attributes

<b>Offset</b>	0x11B4
<b>Type</b>	Read-only
<b>Reset</b>	0x00004000
<b>Width</b>	32

#### 3.3.407 cke\_remap\_control\_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cke\_remap\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11C0
<b>Type</b>	Read-only
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.408 rst\_remap\_control\_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rst\_remap\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11C4
<b>Type</b>	Read-only
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.409 ck\_remap\_control\_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The ck\_remap\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11C8
<b>Type</b>	Read-only
<b>Reset</b>	0x76543210
<b>Width</b>	32

### 3.3.410 power\_group\_control\_31\_00\_now

Power Group Control register for power managing ranks together. The ranks that are CKE-tied together as represented in cke\_remap\_control register should belong to the same power-group Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power\_group\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11D0
<b>Type</b>	Read-only
<b>Reset</b>	0x00020001
<b>Width</b>	32

#### 3.3.411 power\_group\_control\_63\_32\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power\_group\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11D4
<b>Type</b>	Read-only
<b>Reset</b>	0x00080004
<b>Width</b>	32

#### 3.3.412 power\_group\_control\_95\_64\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power\_group\_control\_95\_64\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11D8
<b>Type</b>	Read-only
<b>Reset</b>	0x00200010
<b>Width</b>	32

#### 3.3.413 power\_group\_control\_127\_96\_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power\_group\_control\_127\_96\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x11DC
<b>Type</b>	Read-only
<b>Reset</b>	0x00800040

**Width** 32

### 3.3.414 **feature\_control\_now**

Control register for DMC features. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The feature\_control\_now register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

**Offset** 0x11F0  
**Type** Read-only  
**Reset** 0x0AA00000  
**Width** 32

### 3.3.415 **mux\_control\_now**

Control muxing options for the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The mux\_control\_now register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

**Offset** 0x11F4  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.416 **rank\_remap\_control\_now**

Control register for rank remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rank\_remap\_control\_now register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

**Offset** 0x11F8  
**Type** Read-only  
**Reset** 0x76543210  
**Width** 32

### 3.3.417 t\_refi\_now

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_refi\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1200
<b>Type</b>	Read-only
<b>Reset</b>	0x00090100
<b>Width</b>	32

### 3.3.418 t\_rfc\_now

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rfc\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1204
<b>Type</b>	Read-only
<b>Reset</b>	0x00008C23
<b>Width</b>	32

### 3.3.419 t\_mrr\_now

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_mrr\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1208
<b>Type</b>	Read-only
<b>Reset</b>	0x00000002
<b>Width</b>	32

### 3.3.420 t\_mrw\_now

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_mrw\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x120C
<b>Type</b>	Read-only
<b>Reset</b>	0x0000000C
<b>Width</b>	32

### 3.3.421 t\_rcd\_now

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rcd\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1218
<b>Type</b>	Read-only
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.422 t\_ras\_now

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_ras\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x121C
<b>Type</b>	Read-only
<b>Reset</b>	0x0000000E
<b>Width</b>	32

### 3.3.423 t\_rp\_now

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rp\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1220
<b>Type</b>	Read-only
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.424 t\_rpall\_now

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rpall\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1224
<b>Type</b>	Read-only
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.425 t\_rrd\_now

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The \_l and \_s fields apply to the same bank group, a different bank group, and different logical rank, respectively, as described in the DDR4 specification. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rrd\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1228
<b>Type</b>	Read-only
<b>Reset</b>	0x04000404
<b>Width</b>	32

**3.3.426 t\_act\_window\_now**

Configures the tFAW and tMAWi timing parameters. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_act\_window\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x122C
<b>Type</b>	Read-only
<b>Reset</b>	0x03561414
<b>Width</b>	32

**3.3.427 t\_rtr\_now**

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t\_rtr\_s), same chip, same bank group (t\_rtr\_l), different chip-selects (t\_rtr\_cs), and same chip, different logical rank (t\_rtr\_dlr). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rtr\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1234
<b>Type</b>	Read-only
<b>Reset</b>	0x10060404
<b>Width</b>	32

**3.3.428 t\_rtw\_now**

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t\_rtw\_s), same chip, same bank group (t\_rtw\_l), and other chip-selects (t\_rtw\_cs). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rtw\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1238
<b>Type</b>	Read-only
<b>Reset</b>	0x00060606
<b>Width</b>	32



### 3.3.429 t\_rtp\_now

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rtp\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x123C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000004
<b>Width</b>	32

### 3.3.430 t\_wr\_now

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITES, to the same bank. Note: this must take into account CRC timing requirements. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wr\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1244
<b>Type</b>	Read-only
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.431 t\_wtr\_now

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR\_s), same chip, same bank group (t\_WTR\_l), and alternate chip (tWTR\_cs). Note: these must take into account CRC timing requirements. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wtr\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1248
<b>Type</b>	Read-only
<b>Reset</b>	0x00040505
<b>Width</b>	32

**3.3.432 t\_wtw\_now**

Configures the write-to-write timing parameter for same chip, other bank group (t\_wtw\_s), same chip, same bank group (t\_wtw\_l), alternate chip (t\_wtw\_cs) writes, same chip, different logical rank(t\_wtw\_dlr). Note: these must take into account CRC timing requirements. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wtw\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x124C
<b>Type</b>	Read-only
<b>Reset</b>	0x10060404
<b>Width</b>	32

**3.3.433 t\_xmpd\_now**

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_xmpd\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1254
<b>Type</b>	Read-only
<b>Reset</b>	0x000003FF
<b>Width</b>	32

**3.3.434 t\_ep\_now**

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge powerdownrequest and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_ep\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1258
<b>Type</b>	Read-only
<b>Reset</b>	0x00000002
<b>Width</b>	32

**3.3.435 t\_xp\_now**

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t\_xpdll must be greater than or equal to tRCD and tCKE, and t\_xp must be greater than or equal to tMPX\_S. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_xp\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x125C
<b>Type</b>	Read-only
<b>Reset</b>	0x00060002
<b>Width</b>	32

**3.3.436 t\_esr\_now**

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_esr\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1260
<b>Type</b>	Read-only
<b>Reset</b>	0x0000000E
<b>Width</b>	32

**3.3.437 t\_xsr\_now**

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_xsr\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1264
<b>Type</b>	Read-only
<b>Reset</b>	0x05120100
<b>Width</b>	32

**3.3.438 t\_esrck\_now**

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_esrck\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1268
<b>Type</b>	Read-only
<b>Reset</b>	0x00000005
<b>Width</b>	32

**3.3.439 t\_ckxsr\_now**

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_ckxsr\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x126C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000001
<b>Width</b>	32

**3.3.440 t\_cmd\_now**

Configures command signaling timing. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_cmd\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1270
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.441 t\_parity\_now

Parity latencies t\_parinlat and t\_completion. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_parity\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1274
<b>Type</b>	Read-only
<b>Reset</b>	0x00000900
<b>Width</b>	32

### 3.3.442 t\_zqcs\_now

Configures the delay to apply following a ZQC-Short calibration command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_zqcs\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1278
<b>Type</b>	Read-only
<b>Reset</b>	0x00000040
<b>Width</b>	32

### 3.3.443 t\_rw\_odt\_clr\_now

This timing parameter applies extra guard-band between the last issued rd/wr command and potential ZQC, SREF, and MRS commands which are issued automatically by hardware such as tpoll. This may be necessary to prevent overlap of these automated commands with ranks actively participating in non-target rank ODT (while other ranks are streaming data). ZQC, MRS, and SREF commands are typically not allowed on non-target ranks in this case as these commands could change ODT settings. In general, if non-target rank termination is used this parameter should be programmed to t\_odt\_off\_rd/wr(max setting) + DODTLoff(from DDR4 spec) Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rw\_odt\_clr\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x127C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.444 t\_rddata\_en\_now

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi\_read\_en signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rddata\_en\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1300
<b>Type</b>	Read-only
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.445 t\_phyrdlat\_now

Determines the maximum possible time between the assertion of the dfi\_read\_en signal, and the assertion of the dfi\_rddata\_valid signal by the PHY. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_phyrdlat\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1304
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.446 t\_phywrlat\_now

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi\_wrdata\_en, dfi\_wrdata\_cs and dfi\_wrdata signals. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_phywrlat\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1308
<b>Type</b>	Read-only
<b>Reset</b>	0x00000001
<b>Width</b>	32

### 3.3.447 rdlvl\_control\_now

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rdlvl\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1310
<b>Type</b>	Read-only
<b>Reset</b>	0x00001080
<b>Width</b>	32

### 3.3.448 rdlvl\_mrs\_now

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl\_control register. See the PHY interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rdlvl\_mrs\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1314
<b>Type</b>	Read-only
<b>Reset</b>	0x00000004
<b>Width</b>	32

### 3.3.449 t\_rdlvl\_en\_now

Configures the t\_rdlvl\_en timing parameter. This specifies the cycle delay between asserting dfi\_rdlvl\_en and the first training command, and also the cycle delay between deasserting dfi\_rdlvl\_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rdlvl\_en\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1318
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.450 t\_rdlvl\_rr\_now**

Configures the t\_rdlvl\_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi\_rdlvl\_en after observing dfi\_rdlvl\_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_rdlvl\_rr\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x131C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.451 wrlvl\_control\_now**

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wrlvl\_control\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1320
<b>Type</b>	Read-only
<b>Reset</b>	0x00101000
<b>Width</b>	32

**3.3.452 wrlvl\_mrs\_now**

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl\_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wrlvl\_mrs\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1324
<b>Type</b>	Read-only
<b>Reset</b>	0x00000086
<b>Width</b>	32



**3.3.453 t\_wrlvl\_en\_now**

Configures the t\_wrlvl\_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi\_wrlvl\_en, the delay between asserting dfi\_wrlvl\_en and the first training command, the delay between deasserting dfi\_wrlvl\_en and deasserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wrlvl\_en\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1328
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.454 t\_wrlvl\_ww\_now**

Configures the t\_wrlvl\_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and deasserting dfi\_wrlvl\_en on observing dfi\_wrlvl\_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wrlvl\_ww\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x132C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.455 phy\_power\_control\_now**

Configures the low-power requests made to the PHY for the different channel states. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phy\_power\_control\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1348
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.456 t\_lpresp\_now

Configures the minimum cycle delay to apply for PHY low-power handshakes. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_lpresp\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x134C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.457 phy\_update\_control\_now

Configures the update mechanism to use in response to PHY training requests. Access restrictions: RO  
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phy\_update\_control\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1350
<b>Type</b>	Read-only
<b>Reset</b>	0x2FE00000
<b>Width</b>	32

### 3.3.458 t\_odth\_now

Configures the ODT8 timing parameter as timed from Write command registered with ODT high  
Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_odth\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1354
<b>Type</b>	Read-only
<b>Reset</b>	0x00000006
<b>Width</b>	32

### 3.3.459 odt\_timing\_now

Configures the ODT on and off timing. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_timing\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1358
<b>Type</b>	Read-only
<b>Reset</b>	0x06000600
<b>Width</b>	32

### 3.3.460 odt\_wr\_control\_31\_00\_now

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_wr\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1360
<b>Type</b>	Read-only
<b>Reset</b>	0x08040201
<b>Width</b>	32

### 3.3.461 odt\_wr\_control\_63\_32\_now

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_wr\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1364
<b>Type</b>	Read-only
<b>Reset</b>	0x80402010
<b>Width</b>	32

### 3.3.462 odt\_rd\_control\_31\_00\_now

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_rd\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1368
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.463 odt\_rd\_control\_63\_32\_now

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_rd\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x136C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.464 dq\_map\_control\_15\_00\_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq\_map\_control\_15\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1380
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.465 dq\_map\_control\_31\_16\_now**

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq\_map\_control\_31\_16\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1384
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.466 dq\_map\_control\_47\_32\_now**

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq\_map\_control\_47\_32\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1388
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.467 dq\_map\_control\_63\_48\_now**

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq\_map\_control\_63\_48\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x138C
<b>Type</b>	Read-only

**Reset** 0x00000000  
**Width** 32

### 3.3.468 dq\_map\_control\_71\_64\_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq\_map\_control\_71\_64\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x1390  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.469 odt\_cp\_control\_31\_00\_now

Determines which of the 8 dfi\_odt[7:0] output signals are connected to a logically addressed rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_cp\_control\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x13B0  
**Type** Read-only  
**Reset** 0x08040201  
**Width** 32

### 3.3.470 odt\_cp\_control\_63\_32\_now

Determines which of the 8 dfi\_odt[7:0] output signals are driven during a write to DRAM. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt\_cp\_control\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x13B4  
**Type** Read-only  
**Reset** 0x80402010

**Width** 32

### 3.3.471 user\_config0\_now

Drives the output user\_config0 signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The user\_config0\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x1408  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.472 user\_config1\_now

Drives the output user\_config1 signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The user\_config1\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x140C  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

### 3.3.473 t\_db\_train\_resp\_now

Configures the t\_db\_train\_resp timing parameter for DB-DRAM Training. With DFI4.0 PHY this register is specified to define the cycle delay between DFI read command and when the response is valid on the dfi\_db\_train\_resp. However this register can also be configured in DFI3.1 mode (optional: in absence of dfi\_rddata\_valid) to define the delay between DFI read command and when the response is valid on the dfi\_rddata. This must include the whole round trip time including the board delays, take a look at DFI4.0 spec for details. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_db\_train\_resp\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

**Offset** 0x1610  
**Type** Read-only  
**Reset** 0x00000000  
**Width** 32

**3.3.474 t\_lvl\_disconnect\_now**

Configures the t\_lvl\_disconnect timing parameter for all DFI training interfaces. This value should be programmed to be max of all t\*lvl\_disconnect and t\*lvl\_disconnect\_error timing parameters from the PHY Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_lvl\_disconnect\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1614
<b>Type</b>	Read-only
<b>Reset</b>	0x0000000F
<b>Width</b>	32

**3.3.475 wdqlvl\_control\_now**

Determines the DMC behavior during write-DQ training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl\_control\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1620
<b>Type</b>	Read-only
<b>Reset</b>	0x00000094
<b>Width</b>	32

**3.3.476 wdqlvl\_vrefdq\_train\_mrs\_now**

Determines the Mode Register command to use to place the DRAM into a VrefDQ training mode as part of WrDQ training, when enabled by the wdqlvl\_control register. You enable this function with the wdqlvl\_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl\_vrefdq\_train\_mrs\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1624
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32



### 3.3.477 wdqlvl\_address\_31\_00\_now

Programs the row and column address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl\_address\_31\_00\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1628
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.478 wdqlvl\_address\_63\_32\_now

Programs the address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl\_address\_63\_32\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x162C
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.479 t\_wdqlvl\_en\_now

Configures the t\_wdqlvl\_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi\_wdqlvl\_en, the delay between asserting dfi\_wdqlvl\_en and the first training command, the delay between deasserting dfi\_wdqlvl\_en and deasserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wdqlvl\_en\_now register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1630
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.480 t\_wdqlvl\_ww\_now**

Configures the t\_wdqlvl\_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and deasserting dfi\_wrlvl\_en on observing dfi\_wdqlvl\_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wdqlvl\_ww\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1634
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.481 t\_wdqlvl\_rw\_now**

Configures the t\_wdqlvl\_rw timing parameter. Specifies the minimum numbers of clock cycles from the last read in a calibration sequence to the first write in the next set of calibration commands. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t\_wdqlvl\_rw\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1638
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

**3.3.482 phymstr\_control\_now**

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phymstr\_control\_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

<b>Offset</b>	0x1654
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.483 **periph\_id\_4**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph\_id\_4 register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

<b>Offset</b>	0x1FD0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000014
<b>Width</b>	32

### 3.3.484 **periph\_id\_0**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph\_id\_0 register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

<b>Offset</b>	0x1FE0
<b>Type</b>	Read-only
<b>Reset</b>	0x00000054
<b>Width</b>	32

### 3.3.485 **periph\_id\_1**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph\_id\_1 register characteristics are:

#### **Usage constraints**

There are no usage constraints.

#### **Configurations**

There is only one DMC configuration.

#### **Attributes**

<b>Offset</b>	0x1FE4
<b>Type</b>	Read-only
<b>Reset</b>	0x000000B4
<b>Width</b>	32

### 3.3.486 **periph\_id\_2**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph\_id\_2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1FE8
<b>Type</b>	Read-only
<b>Reset</b>	0x0000000B
<b>Width</b>	32

### 3.3.487 **periph\_id\_3**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph\_id\_3 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1FEC
<b>Type</b>	Read-only
<b>Reset</b>	0x00000000
<b>Width</b>	32

### 3.3.488 **component\_id\_0**

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component\_id\_0 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1FF0
<b>Type</b>	Read-only
<b>Reset</b>	0x0000000D
<b>Width</b>	32

### 3.3.489 **component\_id\_1**

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component\_id\_1 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1FF4
<b>Type</b>	Read-only
<b>Reset</b>	0x000000F0
<b>Width</b>	32

### 3.3.490 component\_id\_2

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component\_id\_2 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1FF8
<b>Type</b>	Read-only
<b>Reset</b>	0x00000005
<b>Width</b>	32

### 3.3.491 component\_id\_3

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component\_id\_3 register characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

There is only one DMC configuration.

#### Attributes

<b>Offset</b>	0x1FFC
<b>Type</b>	Read-only
<b>Reset</b>	0x000000B1
<b>Width</b>	32

# Appendix A

## Signal Descriptions

This appendix describes the DMC-620 signals.

It contains the following sections:

- [A.1 Signals list on page Appx-A-207.](#)

## A.1 Signals list

DMC signals list that excludes bus interface signals. The bus interface signals are defined by their own bus protocol standard.

The following table shows the Primary clock and reset signals bus list of the DMC.

**Table A-1 DMC Primary clock and reset signals list**

Name	Width	Description
<b>clk</b>		Primary DMC clock
<b>resetn</b>		Primary DMC reset

The following table shows the Divided Primary DMC clock. Edge Synchronous, half the frequency of clk bus list of the DMC.

**Table A-2 DMC Divided Primary DMC clock. Edge Synchronous, half the frequency of clk list**

Name	Width	Description
<b>clkdiv2</b>		Primary DMC clock. Edge Synchronous, half the frequency of clk
<b>resetn</b>		Primary DMC reset

The following table shows the APB clock and reset signals bus list of the DMC.

**Table A-3 DMC APB clock and reset signals list**

Name	Width	Description
<b>pclk</b>		APB clock
<b>presetn</b>		APB reset

The following table shows the APB Interface bus list of the DMC.

**Table A-4 DMC APB Interface list**

Name	Width	Description
<b>paddr</b>	32	APB address
<b>psel</b>		APB select
<b>penable</b>		APB enable
<b>pwrite</b>		APB write
<b>pwwdata</b>	32	APB write data
<b>pready</b>		APB ready
<b>prdata</b>	32	APB read data
<b>pslverr</b>		APB error signal

The following table shows the DFI Interface bus list of the DMC.

**Table A-5 DMC DFI Interface list**

Name	Width	Description
dfi_address_p0	18	Address to DDR3 PHY
dfi_address_p1	18	Address to DDR3 PHY
dfi_bank_p0	3	Bank Address to PHY
dfi_bank_p1	3	Bank Address to PHY
dfi_ras_n_p0	1	Row address strobe to PHY
dfi_ras_n_p1	1	Row address strobe to PHY
dfi_cas_n_p0	1	Column address strobe to PHY
dfi_cas_n_p1	1	Column address strobe to PHY
dfi_we_n_p0	1	Write enable to PHY
dfi_we_n_p1	1	Write enable to PHY
dfi_cs_p0	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_cs_p1	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_act_n_p0	1	Activate to PHY
dfi_act_n_p1	1	Activate to PHY
dfi_bg_p0	2	Bank group address to PHY
dfi_bg_p1	2	Bank group address to PHY
dfi_cid_p0	3	Chip ID to PHY
dfi_cid_p1	3	Chip ID to PHY
dfi_cke_p0	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_cke_p1	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_odt_p0	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_odt_p1	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_reset_n_p0	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_reset_n_p1	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_parity_in_p0	1	Command parity to PHY
dfi_parity_in_p1	1	Command parity to PHY
dfi_wrdata_en_p0	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_en_p1	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_p0	(DFI_DATA_BITS/2)	Write data to PHY
dfi_wrdata_p1	(DFI_DATA_BITS/2)	Write data to PHY
dfi_wrdata_cs_p0	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_cs_p1	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_mask_p0	(DFI_DATA_BYTES/2)	Write data mask PHY
dfi_wrdata_mask_p1	(DFI_DATA_BYTES/2)	Write data mask PHY
dfi_rddata_en_p0	(DFI_DATA_SLICES)	Enable for read data



**Table A-5 DMC DFI Interface list (continued)**

Name	Width	Description
<b>dfi_rddata_en_p1</b>	(DFI_DATA_SLICES)	Enable for read data
<b>dfi_rddata_p0</b>	(DFI_DATA_BITS/2)	Read data input from PHY
<b>dfi_rddata_p1</b>	(DFI_DATA_BITS/2)	Read data input from PHY
<b>dfi_rddata_dbi_p0</b>	(DFI_DATA_SLICES*2)	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.
<b>dfi_rddata_dbi_p1</b>	(DFI_DATA_SLICES*2)	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.
<b>dfi_rddata_valid_p0</b>	(DFI_DATA_SLICES)	Indicates read data valid
<b>dfi_rddata_valid_p1</b>	(DFI_DATA_SLICES)	Indicates read data valid
<b>dfi_rddata_cs_p0</b>	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
<b>dfi_rddata_cs_p1</b>	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
<b>dfi_ctrlupd_req</b>	1	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_ctrlupd_ack</b>	1	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_phyupd_req</b>	1	DFI PHY-initiated update request
<b>dfi_phyupd_ack</b>	1	DFI PHY-initiated update acknowledge
<b>dfi_phyupd_type</b>	2	DFI PHY-initiated update type
<b>dfi_data_byte_disable</b>	(DFI_DATA_BYTES/2)	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_dram_clk_disable</b>	MEMORY_CHIP_SELECTS	DRAM clock disable to PHY
<b>dfi_init_start</b>	1	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_init_complete</b>	1	Indicates PHY initialization complete
<b>dfi_alert_n_p0</b>	1	This signal is part of DFI 4.0, see JEDEC specification for details.
<b>dfi_alert_n_p1</b>	1	This signal is part of DFI 4.0, see JEDEC specification for details.
<b>dfi_frequency</b>	5	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_geardown_en</b>	1	This signal is part of DFI 4.0 Geardown Interface.
<b>dfi_err</b>	1	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_err_info</b>	4	This signal is part of DFI 4.0, see DFI specification for details.
<b>dfi_disconnect_error</b>	1	Provides Disconnect type if a disconnect occurs on training, update, or PHY-master interface. This signal is part of DFI 4.0 Disconnect Interface.

**Table A-5 DMC DFI Interface list (continued)**

Name	Width	Description
dfi_phymstr_req	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_cs_state	MEMORY_CHIP_SELECTS	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_state_sel	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_type	2	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phymstr_ack	1	This signal is part of DFI 4.0, see DFI specification for details.
dfi_phylvl_req_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.1, see DFI specification for details.
dfi_phylvl_ack_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.1, see DFI specification for details.
dfi_rdlvl_req	DFI_DATA_SLICES	DFI read data eye training request
dfi_rdlvl_cs	MEMORY_CHIP_SELECTS	DFI read data eye training request target chip-select
dfi_rdlvl_en	DFI_DATA_SLICES	DFI read data eye training enable
dfi_rdlvl_resp	(DFI_DATA_SLICES*2)	DFI read data eye training response
dfi_rdlvl_done	DFI_DATA_SLICES	DFI Read data eye training done
dfi_rdlvl_gate_req	DFI_DATA_SLICES	DFI read gate training request
dfi_rdlvl_gate_cs	MEMORY_CHIP_SELECTS	DFI read gate training request target chip-select
dfi_rdlvl_gate_en	DFI_DATA_SLICES	DFI read gate training enable
dfi_wrlvl_req	DFI_DATA_SLICES	DFI write leveling training request
dfi_wrlvl_cs	MEMORY_CHIP_SELECTS	DFI write leveling training request target chip-select
dfi_wrlvl_en	DFI_DATA_SLICES	DFI write leveling training enable
dfi_wrlvl_strobe_p0	DFI_DATA_SLICES	DFI write leveling training strobe
dfi_wrlvl_strobe_p1	DFI_DATA_SLICES	DFI write leveling training strobe
dfi_wrlvl_resp	DFI_DATA_SLICES	DFI write leveling training response
dfi_wdqlvl_req	DFI_DATA_SLICES	DFI Write-DQ leveling training request
dfi_wdqlvl_cs	MEMORY_CHIP_SELECTS	DFI Write-DQ leveling training request target chip-select
dfi_wdqlvl_en	DFI_DATA_SLICES	DFI Write-DQ leveling training enable
dfi_wdqlvl_result	DFI_DATA_SLICES	DFI Write-DQ leveling training result
dfi_wdqlvl_done	DFI_DATA_SLICES	DFI Write-DQ leveling training done
dfi_wdqlvl_resp	(DFI_DATA_SLICES*2)	DFI Write-DQ leveling training response
dfi_lvl_pattern	4	This signal is part of DFI 4.0, see DFI specification for details.
dfi_lvl_periodic	1	This signal is part of DFI 4.0, see DFI specification for details.

**Table A-5 DMC DFI Interface list (continued)**

Name	Width	Description
<b>dfi_db_train_en</b>	DFI_DATA_SLICES	Enable for DB-DRAM Training. This signal is part of DFI 4.0 DB-DRAM Training.
<b>dfi_db_train_resp_w0</b>	(DFI_DATA_SLICES*DFI_SLICE_WIDTH/4)	Response data for DB-DRAM Training. This signal is part of DFI 4.0.
<b>dfi_db_train_resp_w1</b>	(DFI_DATA_SLICES*DFI_SLICE_WIDTH/4)	Response data for DB-DRAM Training. This signal is part of DFI 4.0.
<b>dfi_lp_ctrl_req</b>	1	DFI command low-power request
<b>dfi_lp_data_req</b>	1	DFI data low-power request
<b>dfi_lp_wakeup</b>	4	DFI command low-power PHY wakeup allowance
<b>dfi_lp_ack</b>	1	DFI command low-power acknowledge

The following table shows the Q-Channel Interface for DMC bus list of the DMC.

**Table A-6 DMC Q-Channel Interface for DMC list**

Name	Width	Description
<b>qreqn</b>	1	Request from the external clock controller to prepare to stop the clock
<b>qacceptn</b>	1	Positive acknowledgement after receiving QREQn assertion indicating that the DMC has completed preparation to stop the clocks and that the external clock controller can stop the clock
<b>qdeny</b>	1	Negative acknowledgement after receiving QREQn assertion indicating that the DMC has refused the request from the external clock controller to prepare to stop the clock
<b>qactive</b>	1	Indication that the DMC is active

The following table shows the Q-Channel Interface for APB interface bus list of the DMC.

**Table A-7 DMC Q-Channel Interface for APB interface list**

Name	Width	Description
<b>qreqn_apb</b>	1	Request from the external clock controller to prepare to stop the clock
<b>qacceptn_apb</b>	1	Positive acknowledgement after receiving QREQn assertion indicating that the APB interface has completed preparation to stop the clocks and that the external clock controller can stop the clock
<b>qdeny_apb</b>	1	Negative acknowledgement after receiving QREQn assertion indicating that the APB interface has refused the request from the external clock controller to prepare to stop the clock
<b>qactive_apb</b>	1	Indication that the APB interface is active

The following table shows the Clock Frequency Change Interface bus list of the DMC.

**Table A-8 DMC Clock Frequency Change Interface list**

Name	Width	Description
<b>cc_frequency</b>	5	Used to indicate new frequency as part of frequency change protocol
<b>cc_freq_change_req</b>	1	Signals to an external clock control that the clock frequency can be updated
<b>cc_freq_change_ack</b>	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Clock Frequency Change Interface bus list of the DMC.

**Table A-9 DMC Clock Frequency Change Interface list**

Name	Width	Description
<b>dfi_frequency</b>	5	Used to indicate new frequency as part of frequency change protocol
<b>dfi_freq_change_req</b>	1	Signals to an external clock control that the clock frequency can be updated
<b>dfi_freq_change_ack</b>	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Abort Interface bus list of the DMC.

**Table A-10 DMC Abort Interface list**

Name	Width	Description
<b>abort_req</b>	1	An input to abort retries in the face of DFI link errors.
<b>abort_err_type</b>	1	Abort Error Type as a payload to abort_req.
<b>abort_ack</b>	1	An output to acknowledge that the DMC has completed outstanding transactions as a result of an abort.

The following table shows the Memory BIST interface bus list of the DMC.

**Table A-11 DMC Memory BIST interface list**

Name	Width	Description
<b>mbistresetn</b>	1	MBIST reset. Active low.
<b>mbistreq</b>	1	MBIST request
<b>mbistack</b>	1	MBIST acknowledge
<b>mbistwriten</b>	1	MBIST write enable
<b>mbistreaden</b>	1	MBIST read enable
<b>mbistaddr</b>	MAX_TID_BITS	MBIST address
<b>mbistarray</b>	4	MBIST array selection
<b>mbistcfg</b>	1	MBIST Configuration
<b>mbistindata</b>	154	MBIST write data
<b>mbistoutdata</b>	154	MBIST read data

The following table shows the DFT interface bus list of the DMC.

**Table A-12 DMC DFT interface list**

Name	Width	Description
<b>DFTCLKGEN</b>	1	DFT clock gate override
<b>DFTRSTDISABLE</b>	2	DFT reset synchronizer disable
<b>DFTRAMHOLD</b>	1	DFT on-chip RAM hold
<b>DFTMCPHOLD</b>	1	DFT multicycle path hold

The following table shows the user-defined inputs bus list of the DMC.

**Table A-13 DMC user-defined inputs list**

Name	Width	Description
user_status	32	User-defined inputs

The following table shows the user-defined outputs bus list of the DMC.

**Table A-14 DMC user-defined outputs list**

Name	Width	Description
user_config0	32	User-defined outputs

The following table shows the user-defined outputs bus list of the DMC.

**Table A-15 DMC user-defined outputs list**

Name	Width	Description
user_config1	32	User-defined outputs

The following table shows the user-defined outputs bus list of the DMC.

**Table A-16 DMC user-defined outputs list**

Name	Width	Description
user_config2	32	User-defined outputs

The following table shows the user-defined outputs bus list of the DMC.

**Table A-17 DMC user-defined outputs list**

Name	Width	Description
user_config3	32	User-defined outputs

The following table shows the Direct command event trigger inputs bus list of the DMC.

**Table A-18 DMC Direct command event trigger inputs list**

Name	Width	Description
direct_cmd_event_in	4	Direct command event trigger inputs

The following table shows the Direct command event triggered outputs bus list of the DMC.

**Table A-19 DMC Direct command event triggered outputs list**

Name	Width	Description
direct_cmd_event_out	4	Direct command event triggered outputs

The following table shows the memory\_type bus list of the DMC.

**Table A-20 DMC memory\_type list**

Name	Width	Description
memory_type	3	An external output of the value of the memory_type register bitfield.

The following table shows the Tie-off value to set the value of CMOD in the periph\_id\_3 bitfield bus list of the DMC.

**Table A-21 DMC Tie-off value to set the value of CMOD in the periph\_id\_3 bitfield list**

Name	Width	Description
user_periph_id_3	8	Tie-off value to set the value of CMOD in the periph_id_3 bitfield

The following table shows the Tie-off value for reset of register bitfield t\_rddata\_en\_diff bus list of the DMC.

**Table A-22 DMC Tie-off value for reset of register bitfield t\_rddata\_en\_diff list**

Name	Width	Description
t_rddata_en_diff_tie_off	6	Tie-off value for reset of register bitfield t_rddata_en_diff

The following table shows the Tie-off value for reset of register bitfield t\_phyrdcslat bus list of the DMC.

**Table A-23 DMC Tie-off value for reset of register bitfield t\_phyrdcslat list**

Name	Width	Description
t_phyrdcslat_tie_off	5	Tie-off value for reset of register bitfield t_phyrdcslat

The following table shows the Tie-off value for reset of register bitfield t\_phyrdlat bus list of the DMC.

**Table A-24 DMC Tie-off value for reset of register bitfield t\_phyrdlat list**

Name	Width	Description
t_phyrdlat_tie_off	7	Tie-off value for reset of register bitfield t_phyrdlat

The following table shows the Tie-off value for reset of register bitfield t\_phywrlat\_diff bus list of the DMC.

**Table A-25 DMC Tie-off value for reset of register bitfield t\_phywrlat\_diff list**

Name	Width	Description
t_phywrlat_diff_tie_off	5	Tie-off value for reset of register bitfield t_phywrlat_diff

The following table shows the Tie-off value for reset of register bitfield t\_phywrcslat bus list of the DMC.

**Table A-26 DMC Tie-off value for reset of register bitfield t\_phywrcslat list**

Name	Width	Description
t_phywrcslat_tie_off	5	Tie-off value for reset of register bitfield t_phywrcslat

The following table shows the Tie-off value for reset of register bitfield t\_phywrdata bus list of the DMC.

**Table A-27 DMC Tie-off value for reset of register bitfield t\_phywrdata list**

Name	Width	Description
t_phywrdata_tie_off	1	Tie-off value for reset of register bitfield t_phywrdata

The following table shows the Tie-off value for reset of register bitfield refresh\_dur\_rdlvl bus list of the DMC.

**Table A-28 DMC Tie-off value for reset of register bitfield refresh\_dur\_rdlvl list**

Name	Width	Description
refresh_dur_rdlvl_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_rdlvl

The following table shows the Tie-off value for reset of register bitfield t\_rdlvl\_en bus list of the DMC.

**Table A-29 DMC Tie-off value for reset of register bitfield t\_rdlvl\_en list**

Name	Width	Description
t_rdlvl_en_tie_off	6	Tie-off value for reset of register bitfield t_rdlvl_en

The following table shows the Tie-off value for reset of register bitfield t\_rdlvl\_rr bus list of the DMC.

**Table A-30 DMC Tie-off value for reset of register bitfield t\_rdlvl\_rr list**

Name	Width	Description
t_rdlvl_rr_tie_off	10	Tie-off value for reset of register bitfield t_rdlvl_rr

The following table shows the Tie-off value for reset of register bitfield refresh\_dur\_wrlvl bus list of the DMC.

**Table A-31 DMC Tie-off value for reset of register bitfield refresh\_dur\_wrlvl list**

Name	Width	Description
refresh_dur_wrlvl_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_wrlvl

The following table shows the Tie-off value for reset of register bitfield t\_wrlvl\_en bus list of the DMC.

**Table A-32 DMC Tie-off value for reset of register bitfield t\_wrlvl\_en list**

Name	Width	Description
t_wrlvl_en_tie_off	6	Tie-off value for reset of register bitfield t_wrlvl_en

The following table shows the Tie-off value for reset of register bitfield t\_wrlvl\_ww bus list of the DMC.

**Table A-33 DMC Tie-off value for reset of register bitfield t\_wrlvl\_ww list**

Name	Width	Description
t_wrlvl_ww_tie_off	10	Tie-off value for reset of register bitfield t_wrlvl_ww

The following table shows the Tie-off value for reset of register bitfield refresh\_dur\_wrlvl bus list of the DMC.

**Table A-34 DMC Tie-off value for reset of register bitfield refresh\_dur\_wrlvl list**

Name	Width	Description
refresh_dur_wdqlvl_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_wrlvl

The following table shows the Tie-off value for reset of register bitfield t\_wdqlvl\_ww bus list of the DMC.

**Table A-35 DMC Tie-off value for reset of register bitfield t\_wdqlvl\_ww list**

Name	Width	Description
t_wdqlvl_ww_tie_off	10	Tie-off value for reset of register bitfield t_wdqlvl_ww

The following table shows the Tie-off value for reset of register bitfield t\_wdqlvl\_rw bus list of the DMC.

**Table A-36 DMC Tie-off value for reset of register bitfield t\_wdqlvl\_rw list**

Name	Width	Description
t_wdqlvl_rw_tie_off	10	Tie-off value for reset of register bitfield t_wdqlvl_rw

The following table shows the Tie-off value for reset of register bitfield t\_wdqlvl\_en bus list of the DMC.

**Table A-37 DMC Tie-off value for reset of register bitfield t\_wdqlvl\_en list**

Name	Width	Description
t_wdqlvl_en_tie_off	6	Tie-off value for reset of register bitfield t_wdqlvl_en

The following table shows the Tie-off value for reset of register bitfield refresh\_dur\_phymstr bus list of the DMC.

**Table A-38 DMC Tie-off value for reset of register bitfield refresh\_dur\_phymstr list**

Name	Width	Description
refresh_dur_phymstr_tie_off	1	Tie-off value for reset of register bitfield refresh_dur_phymstr

The following table shows the Tie-off value for reset of register bitfield t\_db\_train\_resp bus list of the DMC.

**Table A-39 DMC Tie-off value for reset of register bitfield t\_db\_train\_resp list**

Name	Width	Description
t_db_train_resp_tie_off	7	Tie-off value for reset of register bitfield t_db_train_resp

The following table shows the Tie-off value for reset of register bitfield t\_lpresp bus list of the DMC.



**Table A-40 DMC Tie-off value for reset of register bitfield t\_lpresp list**

Name	Width	Description
t_lpresp_tie_off	6	Tie-off value for reset of register bitfield t_lpresp

The following table shows the Tie-off value for reset of register bitfield user\_config0 bus list of the DMC.

**Table A-41 DMC Tie-off value for reset of register bitfield user\_config0 list**

Name	Width	Description
user_config0_tie_off	32	Tie-off value for reset of register bitfield user_config0

The following table shows the Tie-off value for reset of register bitfield user\_config1 bus list of the DMC.

**Table A-42 DMC Tie-off value for reset of register bitfield user\_config1 list**

Name	Width	Description
user_config1_tie_off	32	Tie-off value for reset of register bitfield user_config1

The following table shows the Tie-off value for reset of register bitfield user\_config2 bus list of the DMC.

**Table A-43 DMC Tie-off value for reset of register bitfield user\_config2 list**

Name	Width	Description
user_config2_tie_off	32	Tie-off value for reset of register bitfield user_config2

The following table shows the Tie-off value for reset of register bitfield user\_config3 bus list of the DMC.

**Table A-44 DMC Tie-off value for reset of register bitfield user\_config3 list**

Name	Width	Description
user_config3_tie_off	32	Tie-off value for reset of register bitfield user_config3

The following table shows the Tie-off value to set the physical node ID of the DMC bus list of the DMC.

**Table A-45 DMC Tie-off value to set the physical node ID of the DMC list**

Name	Width	Description
system_id	CHI_RSP_FLIT_SRCID_WIDTH	Tie-off value to set the physical node ID of the DMC

The following table shows the Tie off value to specify the concatenated physical node IDs of up to SYSTEM\_REQUESTORS Home Nodes that are permitted to access the DMC. SYSTEM\_REQUESTORS is 8 when configured as DMC\_CHIB==0, and is 32 when configured as DMC\_CHIB==1. Bus list of the DMC.

Access the DMC. **SYSTEM\_REQUESTORS** is 8 when configured as **DMC\_CHIB==0**, and is 32 when configured as **DMC\_CHIB==1**. list

Name	Width	Description
<b>home_node_id</b>	(CHI_REQ_FLIT_SRCID_WIDTH*SYSTEM_REQUESTORS)	Tie off value to specify the concatenated physical node IDs of the requestors that are permitted to access the DMC

The following table shows the Tie-off value to set the value for **dfi\_lvl\_periodic** when a **dfi\_rdlvl\_req** is occurring bus list of the DMC.

**Table A-47 DMC Tie-off value to set the value for dfi\_lvl\_periodic when a dfi\_rdlvl\_req is occurring list**

Name	Width	Description
<b>dfi_rdlvl_periodic</b>	1	Tie-off value to set the value for <b>dfi_lvl_periodic</b> when a <b>dfi_rdlvl_req</b> is occurring

The following table shows the Tie-off value to set the value for **dfi\_lvl\_periodic** when a **dfi\_rdlvl\_gate\_req** is occurring bus list of the DMC.

**Table A-48 DMC Tie-off value to set the value for dfi\_lvl\_periodic when a dfi\_rdlvl\_gate\_req is occurring list**

Name	Width	Description
<b>dfi_rdlvl_gate_periodic</b>	1	Tie-off value to set the value for <b>dfi_lvl_periodic</b> when a <b>dfi_rdlvl_gate_req</b> is occurring

The following table shows the Tie-off value to set the value for **dfi\_lvl\_periodic** when a **dfi\_wrlvl\_req** is occurring bus list of the DMC.

**Table A-49 DMC Tie-off value to set the value for dfi\_lvl\_periodic when a dfi\_wrlvl\_req is occurring list**

Name	Width	Description
<b>dfi_wrlvl_periodic</b>	1	Tie-off value to set the value for <b>dfi_lvl_periodic</b> when a <b>dfi_wrlvl_req</b> is occurring

The following table shows the Tie-off value to set the value for **dfi\_lvl\_periodic** when a **dfi\_wdqlvl\_req** is occurring bus list of the DMC.

**Table A-50 DMC Tie-off value to set the value for dfi\_lvl\_periodic when a dfi\_wdqlvl\_req is occurring list**

Name	Width	Description
<b>dfi_wdqlvl_periodic</b>	1	Tie-off value to set the value for <b>dfi_lvl_periodic</b> when a <b>dfi_wdqlvl_req</b> is occurring

The following table shows the interrupt signal list of the DMC.

**Table A-51 DMC interrupts list**

Name	Width	Description
<b>interrupt_er_Master</b>	1	The DMC has detected an uncorrectable error in an internal RAM
<b>interrupt_cfh_Master</b>	1	The DMC has detected a correctable error
<b>interrupt_fh_Master</b>	1	The DMC has detected a data failure that could not be corrected in a DRAM burst operation
<b>interrupt_failed_access_Master</b>	1	The DMC has detected a system request that has failed a permissions check

**Table A-51 DMC interrupts list (continued)**

Name	Width	Description
<b>interrupt_failed_prog_Master</b>	1	The DMC has detected a programming request that is not permitted
<b>interrupt_link_err_Master</b>	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun
<b>interrupt_temperature_event_Master</b>	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor
<b>interrupt_arch_fsm_Master</b>	1	The DMC has detected a change in the architectural state.
<b>interrupt_scrub_engine0_complete_Master</b>	1	The DMC scrub engine 0 has completed a scrub.
<b>interrupt_scrub_engine1_complete_Master</b>	1	The DMC scrub engine 1 has completed a scrub.
<b>interrupt_scrub_engine_behind_schedule_Master</b>	1	A DMC scrub engine is behind schedule.
<b>interrupt_phy_request_Master</b>	1	The DMC has detected a PHY request.
<b>interrupt_combined_Master</b>	1	A combined interrupt that is the logical OR of the other interrupts.
<b>interrupt_failed_access_oflow_Master</b>	1	The DMC has detected a system request that has failed a permissions check and a previously detected assertion was not cleared.
<b>interrupt_failed_prog_oflow_Master</b>	1	The DMC has detected a programming request that is not permitted and a previously detected assertion was not cleared.
<b>interrupt_link_err_oflow_Master</b>	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun and a previously detected assertion was not cleared.
<b>interrupt_temperature_event_oflow_Master</b>	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor and a previously detected assertion was not cleared.
<b>interrupt_arch_fsm_oflow_Master</b>	1	The DMC has detected a change in the architectural state and a previously detected assertion was not cleared.
<b>interrupt_scrub_engine0_complete_oflow_Master</b>	1	The DMC scrub engine 0 has completed a scrub and a previously detected assertion was not cleared
<b>interrupt_scrub_engine1_complete_oflow_Master</b>	1	The DMC scrub engine 1 has completed a scrub and a previously detected assertion was not cleared
<b>interrupt_scrub_engine_behind_schedule_oflow_Master</b>	1	A DMC scrub engine is behind schedule and a previously detected assertion was not cleared.
<b>interrupt_phy_request_oflow_Master</b>	1	The DMC has detected a PHY request and a previously detected assertion was not cleared.
<b>interrupt_combined_oflow_Master</b>	1	A combined interrupt that is the logical OR of the other interrupt overflows.
<b>interrupt_pmu_counter_oflow_Master</b>	1	An interrupt that indicates at least one PMU counter has overflowed.

# Appendix B

## Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following sections:

- [B.1 Revisions on page Appx-B-221](#).

## B.1 Revisions

This appendix describes the technical changes between released issues of this book.

**Table B-1 Issue 0000-00**

Change	Location	Affects
First release	-	All revisions.

**Table B-2 Differences between issue 0000-00 and issue 0000-01**

Change	Location	Affects
No technical changes.	-	All revisions.